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Interface studies of ZnO nanowire transistors using low-frequency noise and temperature-dependent *I-V* measurements

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Single ZnO nanowire (NW) transistors fabricated with self-assembled nanodielectric (SAND) and SiO_2 gate insulators were characterized by low-frequency noise and variable temperature current-voltage (*I-V*) measurements. According to the gate dependence of the noise amplitude, the extracted Hooge's constants (α_H) are $\sim 3.3\times 10^{-2}$ for SAND-based devices and $\sim 3.5\times 10^{-1}$ for SiO_2-based devices. Temperature-dependent *I-V* studies show that the hysteresis of the transfer curves and the threshold voltage shifts of SAND-based devices are significantly smaller than those of SiO_2-based devices. These results demonstrate the improved SAND/ZnO NW interface quality (lower interface-trap states and defects) in comparison to those fabricated with SiO_2. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2830005]

Semiconductor nanowire transistors (NWTs) have attracted considerable interest for future electronic and optoelectronic applications. Among the most promising semiconductor nanowire materials, high-performance and reliable ZnO NWTs might enable challenging applications for flexible or/and transparent electronics and bio/chemical sensors. In order to realize devices useful for circuit applications, various device characteristics must be achieved, including high on-current (I_{on}) in order to provide sufficient drive capability and, for digital applications, a small threshold voltage (V_{th}), a steep subthreshold slope (S), and low off-current (I_{off}). In addition to choice of specific channel materials, many other factors may influence device performance, including gate and contact materials, fabrication process factors (thermal annealing, photolithography, etching, implantation, etc.), layout design factors (channel width and length, device structures, etc.), and device operating factors (bias stress, temperature, etc.).[1] Given the relatively large potential influence of interfaces, it is important to control the surface state densities at these interfaces, and to develop methods to quantify their impact on device performance. In addition, NWTs often use metal (Schottky) source/drain contacts deposited directly on the nanowire, instead of doped semiconductor regions that form the local contacts to the channel in complementary metal-oxide semiconductor devices. The realization of high performance devices requires development of metal source/drain (S/D) contacts with low contact resistance, which generally implies a small injection barrier between the metal and the semiconductor channel.

Studies of low-frequency ($1/f$) noise in semiconductor NWTs are of interest both from a standpoint of quantifying device performance for specific applications as well as for determining the densities of surface/interface states in the devices. The quality of the interfaces in NWTs can be judged by noise properties from low frequency noise measurements,[2–5] which are generally sensitive to interface states present along the length of the channel. Comparisons of the noise amplitude in NWTs with that measured for other device structures also allow evaluation of the suitability of NWTs in low-noise applications. Although many other noise mechanisms may contribute to degradation of device performance, $1/f$ noise is important in many applications, since the noise in this spectral range can be upconverted upon mixing or modulation/demodulation of signals and, therefore, can contribute to system noise in other spectral ranges. Temperature-dependent current-voltage (*I-V*) measurements, performed over a range of gate and drain biases, can provide important information about the effective injection barrier between the source metal and the nanowire channel, and can guide development of appropriate contact structures. In this study, we have investigated single ZnO NWTs using self-assembled nanodielectrics (SANDs) and SiO_2 as gate insulators in terms of their low-frequency noise and temperature-dependent current versus voltage (*I-V*) characteristics.

The ZnO nanowires (120 nm average diameter, Nanolab Inc.) were transferred onto Si substrates (back gate) coated with SAND (15 nm)[7] or SiO_2 (40 nm) dielectrics, and Al metal was used for S/D electrodes. The average gate length between source and drain electrodes was $\sim 2\ \mu$m. The single-nanowire devices were passivated with SiO_2 (~ 300 nm) in order to protect the nanowires from ambient. Details of the device structure and fabrication of comparable devices have been reported preciously.[8,9]

Figure 1(a) shows the drain current noise spectrum of a representative SAND-based ZnO NWT as a function of drain bias (V_{ds}) at a gate voltage of 2 V. The increase in drain bias leads to an increase in drain current, due to an increase in the number of carriers per second crossing into the drain, which in turn leads to a higher amplitude of current noise at a specific gate bias. Figure 1(b) shows the current noise spectrum (S_I) at 100 Hz and square of the drain current (I_d^2), plotted versus V_{ds}. The S_I of the NWT is observed to be proportional to the squared drain current (I_d^2) over this range of drain biases as expected from a noise model based on the fluctuation in the number of carriers. Next, the correlation of

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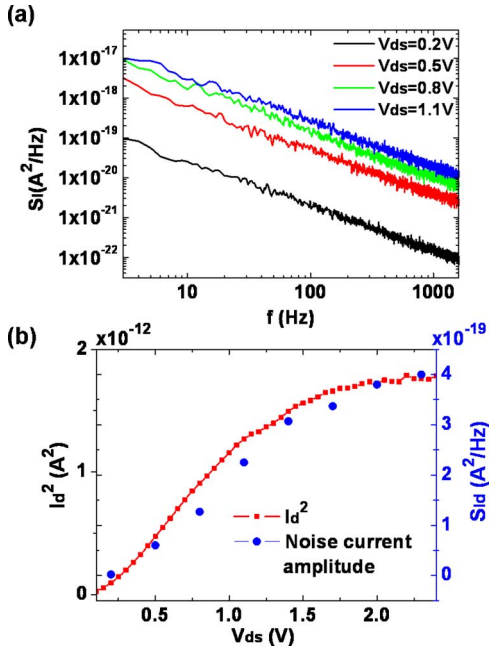

FIG. 1. (Color online) (a) Measured drain current noise spectrum of a SAND-based ZnO NWT at V_{ds}=0.2, 0.5, 0.8, and 1.1 V and V_{gs}=2 V. (b) The I_d^2 and amplitude of current noise spectrum at 100 Hz plotted vs V_{ds} at a gate bias of 2 V.

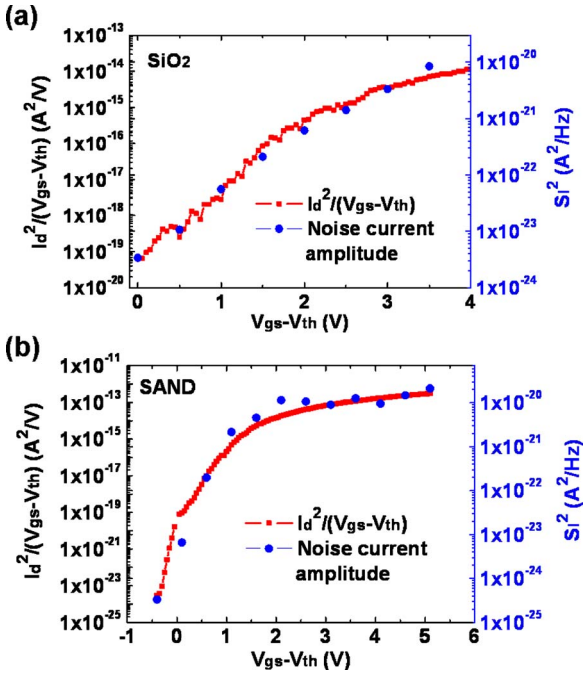

FIG. 2. (Color online) Measured $I_d^2/(V_{gs}\text{-}V_{th})$ and the amplitude of current noise spectrum (S_I) plotted as a function of gate bias at a drain bias of 0.1 V for (a) ZnO/SiO_2 and (b) ZnO/SAND.

drain current (I_d) versus current noise spectrum (S_I) as a function of gate bias, with V_{ds}=0.1 V (transistor linear operating regime), is examined to understand the gate-dependent current noise spectrum. A recent study of low frequency noise in ZnO NWTs has presented a basic model for $1/f$ noise in NWTs.[2] This model is applied here to interpret the interface quality of ZnO NW on SAND as well as on SiO_2. According to Hooge's empirical model,[6] the $1/f$ noise behavior can be described by

$$S_I(f) = \frac{\alpha_H \times I_d^\beta}{f \times N}, \tag{1}$$

where I_d is the drain current, α_H is the Hooge's constant, β is current dependence exponent, and N is the total number of carriers in the channel of the NWT. The value of α_H can be utilized as a parameter to compare interface trap densities in various devices, and allows a direct comparison between the SAND-based and SiO_2-based devices. In the strong inversion region, the total number of carriers in the channel can be calculated using the following equation:[2,4]

$$N = \frac{|V_{gs} - V_{th}|}{q} \times C_g \quad \left(\text{where } C_g = \frac{2\pi\varepsilon\varepsilon_0 L}{\cosh^{-1}(1 + h/r)}\right), \tag{2}$$

where h is the thickness of a gate insulator, L is the gate length (2 μm), and r is the nanowire radius. The calculated gate capacitances for NWTs with the various gate dielectrics C_g (SAND) and C_g (SiO_2) are 4.81×10^{-16} and 3.95×10^{-16} F, respectively. Combining Eqs. (1) and (2), one can calculate the current noise spectrum of a ZnO NW device in the linear operating region as a function of gate voltage,

$$S_I = \frac{AI_d^\beta}{f} = \frac{q\alpha_H I_d^\beta}{|V_{gs} - V_{th}| C_g f} \quad \left(\text{where } \frac{1}{A} = \frac{C_g}{q\alpha_H}|V_{gs} - V_{th}|\right). \tag{3}$$

In order to verify this relationship, Fig. 2 plots the measured S_I and $I_d^2/(V_{gs}\text{-}V_{th})$ versus $(V_{gs}\text{-}V_{th})$ for both the SiO_2-based [Fig. 2(a)] and SAND-based [Fig. 2(b)] ZnO NWTs. The data are observed to follow the relationship predicted by Eq. (3), with β=2.

The extracted α_H values from the data in Fig. 2 and Eq. (3) are $\sim3.3\times10^{-2}$ (ZnO/SAND NWTs) and $\sim3.5\times10^{-1}$ (ZnO/SiO_2 NWTs). We utilized the α_H value as a parameter to compare the interface quality in the respective devices. Since both types of NWTs received the same ozone treatment and passivation, the observation of significantly lower α_H for the ZnO/SAND devices versus the ZnO/SiO_2 devices indicates that the interface between the nanowire and the gate dielectric, rather than the top surface of the nanowire, is the interface primarily responsible for the generation of $1/f$ noise. This reduction also indicates that the SAND provides an interface to the nanowire with a significantly lower interface state density than that present at the nanowire/SiO_2 interface. The observation of reduced $1/f$ noise in ZnO/SAND devices is consistent with prior reports of improved subthreshold slopes and reduced off current levels in ZnO/SAND devices with respect to those in ZnO/SiO_2 devices. Recently, α_H values for carbon nanotude transistors (CNTs) ($\alpha_H\sim9.3\times10^{-3}$) and ZnO NWTs ($\alpha_H\sim5\times10^{-3}$) were measured in ultrahigh vacuum (UHV).[3,6] For the ZnO NWTs, the α_H values in air are 2–4 times larger than those in UHV.[6] The present extracted α_H of SAND-based NWTs in air is comparable to these values. Although semiconductor nanowires could exhibit a large number of dangling bonds or other surface/interface states compared to CNTs, the observation of an α_H value comparable to those observed in CNT transistors implies that the overall surface state densities in the present devices are comparable to those in CNTs.

Information about the contact interfaces can be obtained from studies of the current-voltage characteristics versus temperature. Figure 3 shows the temperature dependence of the transfer curves for representative ZnO NWTs (T_s =25–100 °C in 25 °C steps), measured at V_{ds}=0.1 V. The temperature dependence of the transfer curve can be analyzed by considering three regions: thermal generation re-

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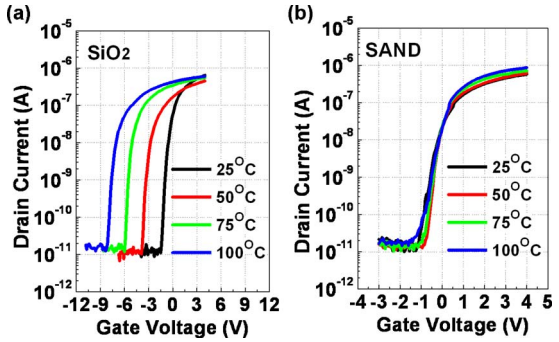

FIG. 3. (Color online) Temperature-dependent I_{ds}-V_{gs} characteristics of (a) ZnO/SiO_2 NWT and (b) ZnO/SAND NWT.

gion, subthreshold region, and on-state region. In the subthreshold region, the drain current increases with temperature because of the existence of a quasi-Fermi level between the intrinsic Fermi level and the bottom of the band tail states. In the on-state region, the drain current does not change significantly because of the low tail state density. The temperature variation of the transfer curves of the ZnO/SiO_2 NWTs shown in Fig. 3(a) is due to charge traps in the SiO_2 gate insulator. On the other hand, the transfer curve of the ZnO/SAND NWTs exhibits a much smaller temperature dependence, which indicates that the density of charge traps in the SAND is small compared to that of the SiO_2 gate insulator. In addition, the relatively constant "off" current indicates that thermal leakage currents, which would be observed as an increasing off current with increasing temperature in the thermal generation region, and which are significant in α-Si transistors and poly-Si transistors, is not a dominant effect here. This indicates that thermal generation of carriers in ZnO NWTs is negligible, as expected based on the relatively large ZnO bandgap ($\sim$3.6 eV). The threshold voltage shifts (ΔV_{th}) versus temperature of the ZnO/SAND NWTs are significantly smaller than those of the ZnO/SiO_2 NWTs. These trends provide further evidence that the SAND-based NWTs have low interface trap and defect densities between the SAND gate dielectric and the ZnO nanowire.

In order to understand the role of contacts on the conduction properties of ZnO nanowires, the temperature-dependent I_{ds}-V_{gs} characteristics of ZnO/SAND NWTs were measured at different gate biases (V_{gs} from -3 to 4 V, 0.05 steps). An Arrhenius plot of $\log I_d$ versus $1000/T$ at V_{ds} $=0.1$ V is shown for various values of V_{gs} in Fig. 4(a). The drain current in log scale is approximately linear versus $1000/T$ from $V_{gs}=-3$ to 4 V. Figure 4(b) shows the activation energy (E_a) inferred from the slopes of the curves in Fig. 4(a), as a function of gate voltage. The extracted activation energy peaks at $V_{gs}<-0.65$ V, slightly below V_{th}, with a value of $\sim$360 meV. For gate voltages just beyond threshold, $E_a\sim 50$ meV, while values approaching 100 meV are observed for bias well above threshold. Figure 4(c) shows an energy band diagram for ZnO NWTs with changing gate bias at 0.1 V_{ds}, qualitatively illustrating the changes in contact to channel barrier. The ZnO electron affinity (χ_{ZnO}) is 4.29 eV and the effective ZnO work function (Φ_{ZnO}) is 4.45 eV for n-type ZnO thin film. Based on the work function of Al ($\Phi_{Al}=4.28$ eV), it is expected that Al S/D contacts form low barrier height interfaces to n-type ZnO. The positive gate bias decreases the electron barrier height (Φ_B), and Φ_B becomes small in the "on" region, whereas negative gate bias should increase Φ_B. Channel activation energies extracted from Arrhenius plots of the SAND-based ZnO NWTs provide information about the relative barriers for charge injection into the channel. The activation energy dependence on gate bias indicates that the contact barriers are relatively low, as would be expected for the small offset between the contact metal (Al) work function and the calculated bulk Fermi level position for the n-type nanowires.

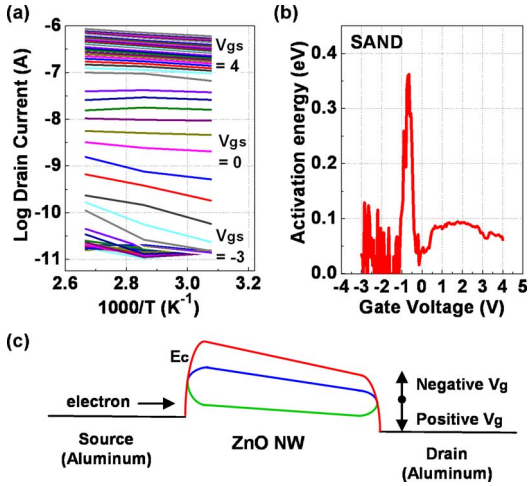

FIG. 4. (Color online) (a) Arrhenius plot. (b) Channel activation energy, inferred from slope of Arrhenius plot vs gate voltage. (c) Energy band diagram at various gate biases ($V_{ds}=0.1$ V).

In conclusion, we investigated interface quality of SAND- and SiO_2-based ZnO NWTs utilizing low frequency noise as a function of gate bias. The lower α_H for SAND-based ZnO NWTs indicates the high quality of the SAND-ZnO NW interface, compared to the SiO_2–ZnO NW interface. Furthermore, single SAND-based ZnO NWTs show stable transistor characteristics in terms of ΔV_{th}, S, and $I_{on}:I_{off}$ as a function of temperature. These results suggest challenging opportunities for implementing robust SANDs in ZnO NWTs to realize high performance and high interface quality.

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