COMMUNICATION

Fully Transparent Thin-Film Transistors Based on Aligned Carbon Nanotube Arrays and Indium Tin Oxide Electrodes

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The development of mechanically flexible and/or optically transparent electronics could enable next-generation electronics technologies, which would be easy-to-read, light-weight, unbreakable, transparent, and flexible. Potential applications could include transparent monitors, heads-up displays, and conformable products. Recent reports have demonstrated transparent thin film transistors (TFTs) using channels consisting of semiconductor nanowires (ZnO, SnO_2, or In_2O_3) and random networks of single-walled carbon nanotubes (SWNTs).[1,2] Transparent TFTs are attractive for the drive circuitry in transparent and/or flexible active matrix display devices. These devices could overcome the limitations of conventional polycrystalline silicon and amorphous silicon thin film transistors, such as low mobility, non-transparency, or high temperature processing.[3–5]

Among these nanowire and nanotube materials, SWNTs could be a strong candidate for integrating high performance transistor circuits while satisfying the requirements for high density nanoscale integration, including ballistic transport, low power consumption, mechanical flexibility, and optical transparency. SWNT field effect transistors (FETs) using Pd source/drain electrodes and high-*k* atomic layer deposition (ALD)-based ZrO_2 and HfO_2 thin films as gate dielectrics have exhibited high performance transistor characteristics, including near ballistic transport and near ideal values of subthreshold slope (S) of ~60 mV/decade in non-hydrogen ambient conditions.[6] Even though SWNT-FETs provide excellent electrical properties, the integration of individual SWNTs has been impeded by uncontrolled variations of SWNT-TFTs, such as variation of chirality and diameter of SWNTs during thermal chemical vapor deposition (CVD) growth, and alignment for device integration. In order to overcome these limits, new approaches for realization of complex circuits have been demonstrated using well-aligned SWNT arrays on insulating substrates, where the average number of assembled nanotubes are uniform from device to device.[7–9] Previous studies involving SWNT networks[2] and other semiconductors[1] have demonstrated highly bendable, transparent TFTs, but the network-based TFTs suffer from relatively low mobility and difficulties in scaling down the channel length, making it difficult to obtain high performance transistors.

Here, we report the first demonstration of fully transparent TFTs based on well-aligned SWNTs arrays, with conduction from source to drain occurring through individual SWNTs, rather than through networks. A recently developed technique for realizing aligned SWNT arrays on quartz substrates[10] is utilized to place SWNTs into a specific area for the active channel layer. Transparent indium tin oxide (ITO) source/drain and gate electrodes provide excellent contacts to the SWNTs, resulting in high performance transistor characteristics. Representative SWNT-TFTs exhibit high performance depletion-mode[11,12] p-type transistor characteristics with ~83% transparency over the visible wavelength range. The fully transparent SWNT-TFTs could be attractive candidates for future flexible and/or transparent electronics.

Figure 1a shows a cross-sectional view of a SWNT-TFT, which employs an aligned array of SWNTs as the active channel, ITO gate, and source/drain electrodes, and a HfO_2 gate dielectric. Prior to growth of SWNTs, a ST-cut quartz substrate is annealed for 8 h at 900 °C in air. SWNTs are synthesized on the annealed quartz substrates by thermal CVD of methane using an iron catalyst. Nearly perfect alignment of SWNTs is achieved with direct growth of nanotubes (Fig. 1b).[10] The insert in Figure 1b is a higher-magnification field emission scanning electron microscopy (FESEM) image, showing the well-aligned SWNTs. The parallel arrays of grown SWNT have diameters of 1–5 nm, and an average density of 0.5 tubes μm^{-1}. The quality of the array could potentially be improved by increasing the annealing time, which might increase the degree of the order in the crystal lattice near the surface. The separation of individual SWNTs in the aligned array avoids junctions within the array, as well as electrostatic screening of the gate field by adjacent SWNTs, resulting in conductance properties per SWNT comparable to studies involving single SWNTs per device.[4,11] This is a significant improvement over previous reported results on random network SWNT transistors.[7] After depositing ITO source/drain electrodes (100 nm) by ion-assisted deposition (IAD)[1] at room temperature, the electrical burning described below is performed

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ADVANCED MATERIALS

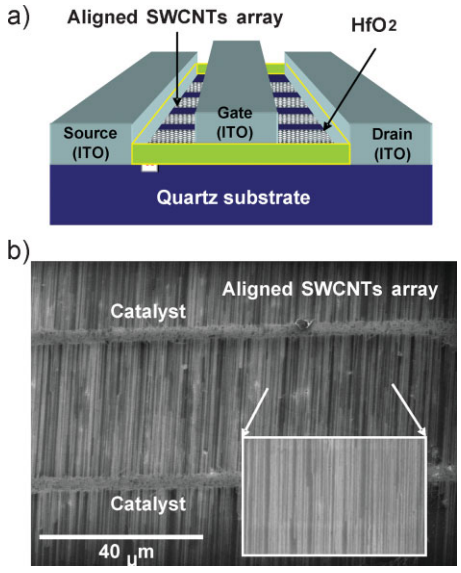

Figure 1. a) Schematic view of a top-gate TFT employing an aligned SWNT array with a HfO_2 gate dielectric. b) SEM image of an aligned array of SWNT-TFT with an inset providing a higher magnification. The array contains ~0.5 SWNTs μm^{-1}.

on the two-terminal device in order to improve the transistor characteristics, especially the on/off current ratio (I_{on}/I_{off}.) A 20 nm high-k HfO_2 film is deposited at 300 °C using precursors of $HfCl_4$ and H_2O in an ASM Micro-chemistry F-120 ALCVD™ Reactor. Top ITO gate electrodes are deposited by IAD and lithographically defined with minimum gate lengths of 2 μm.

The advantages of well-aligned SWNT-TFTs are high mobility and nanoscale integration. Due to the high tunneling resistance of tube–tube crossings in SWNT network devices, the performance of random network SWNT-TFTs is far below the intrinsic characteristics inferred from devices employing single semiconducting SWNTs.[7,15] Moreover, it is typically difficult to scale down the channel length in network devices, since the device characteristics change significantly as the channel length becomes comparable to the average spacing between metallic tubes.[15] The use of a well-aligned SWNT array allows devices in which the current flow is through a number of individual SWNTs, each connected to both the source and drain electrodes. On the other hand, during the thermal growth process, both metallic and semiconducting SWNTs are formed with roughly the expected ratio of 1/3 metallic and 2/3 semiconducting SWNTs.[7] The metallic SWNTs provide a high conductance path between source and drain, resulting in a low I_{on}/I_{off} of 5–10 in devices fabricated without electrical burning.

In order to improve I_{on}/I_{off} for the TFTs, electrical burning (a self-heating due to application of a drain/source bias in air) is performed to remove metallic SWNTs. More than 80% of the designed SWNT-TFTs show $I_{on}/I_{off} > 10^3$ following electrical burning. Figure 2a shows the current versus voltage (I–V) characteristics of a representative two-terminal device during electrical burning at high drain bias while the gate electrode is floating. As the drain voltage and drain current increase, a common dissipative process involving electron-phonon scattering causes self-heating of the SWNTs.[13] The step decreases in

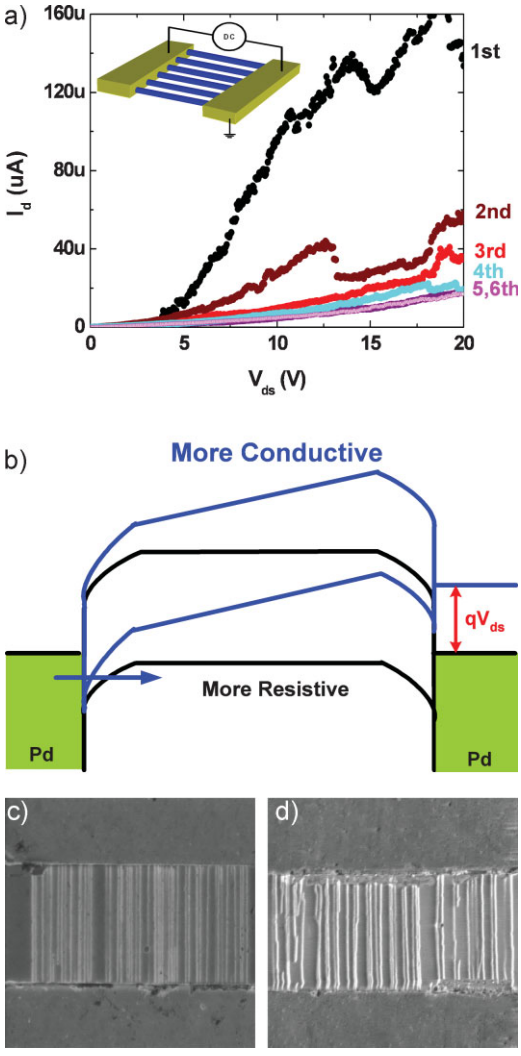

Figure 2. a) I–V characteristics of aligned SWNT arrays under the process of electrical burning as the drain bias is swept from 0 V to 20 V. The inset shows a schematic view of the set-up for electrical burning test. b) Band diagram for a semiconducting SWNT for "more resistive" and "more conductive" states after electrical burning. (black) For low drain bias, a thick Schottky barrier blocks flow of current. (blue) Carriers can cross the thinner Schottky barrier at high drain bias (>5 V). c and d) SEM images of aligned SWNT arrays before and after electrical burning, respectively.

current observed in Figure 2a are associated with the breakdown of individual metallic SWNTs due to local oxidation in air. The sudden increases of current around $V_{ds} = 18$ V for two of the curves are not fully understood, but may be related to local contact annealing as most of the heat is generated near nanotube–ITO contact. By comparing Figures 2c and 2d, it is apparent that most of the burned-out nanotubes break near the nanotube–ITO contacts. Previous reports demonstrate that metallic SWNTs can break down in air for drain/source biases below 15 V, while semiconducting SWNTs have breakdown voltages of ~23 V.[14,15] As shown in Figure 2a, for biases below 20 V, several steps in current are observed, corresponding to the breakdown of a number of metallic SWNTs. For the representative device shown in Figure 2a, breakdown events are observed during the first four

voltage sweeps, but the device characteristics remain nominally constant in subsequent sweeps. Figure 2b shows a schematic energy band-diagram for a two-terminal device containing a semiconducting SWNT with ITO contacts for both the on state and the off state. For low drain/source voltages, the Schottky barrier between the ITO and the SWNT can block the transport of carriers (holes). At higher biases, the Schottky barrier becomes more transparent, and a significant number of holes can tunnel through the barrier. From the 5th and 6th voltage scans during electrical burning, this stability of current is interpreted as corresponding to a condition in which the remaining SWNTs in the TFT are all semiconducting. Following the electrical burning process, the density of SWNTs decreases to approximately 0.25 tubes μm^{-1}. This decrease in density includes those nanotubes burnt locally at their contacts with ITO and does not represent working nanotubes. For devices employing this electrical breakdown processes, more than 80% of the SWNT-TFTs show I_{on}/I_{off} above 10^3.

Figure 3 shows the transistor characteristics for SWNT- TFTs with a gate length of 2 μm and widths (defined by the width of the source and drain contacts) of 6 μm (Figs. 3a–c) and 50 μm (Figs. 3d and 3e). Electrical burning is executed to remove metallic SWNTs at both devices. Figure 3a shows the transfer curves ($V_{ds} = -1$ V) of the single semiconducting SWNT-TFT before and after thermal annealing. An annealing step is carried out after gate deposition in order to reduce the contact resistance between the ITO source/drain electrodes and SWNTs, and interface traps in and on the HfO_2 gate insulator and at the interface between SWNTs and the gate insulator. The post deposition annealing is performed in Ar ambient conditions at 350 °C for 10 min. Through post deposition annealing, the subthreshold slope ($S = dV_{gs}/[d(\log_{10} I_d)]$) is significantly improved from 500 mV/decade to 400 mV/decade. Post deposition annealing reduces the density of interface traps between ITO contact, SWNTs, and oxide, which results in an improved subthreshold slope. Clearly, lower S causes the transistor to ''turn off'' as close to threshold voltage as possible. The gate capacitance per unit length (C_t) yields $2\pi\varepsilon_r\varepsilon_0/\cosh^{-1}(1+h/r)$ presuming a cylindrical tube model, where $\varepsilon_r = 15$ is the effective dielectric constant of HfO_2, h is the oxide layer thickness, and r is the radius of the CNTs.[8,10] A maximum transconductance ($g_m = dI_d/dV_{gs}|_{V_{ds}=-1V}$) of 0.65 μS, a field effect mobility of ~285 $cm^2\ V^{-1}\ s^{-1}$, and I_{on}/I_{off} of $\sim 10^4$ are observed. Note that the gate leakage current is at least six orders of magnitude lower than drain current. Figure 3c shows the drain current versus drain/source voltage (I_d–V_{ds}) characteristics of the SWNT-TFT following the annealing. The device shows a maximum on-current of ~2.5 μA at $V_{ds} = -4$ V and $V_{gs} = -2$V.

Figure 3d shows the I_d–V_{gs} characteristics of a SWNT-TFT with a width of 50 μm, following annealing. Following electrical burning, the channel contains approximately 13 aligned SWNTs. A recent report shows an average per tube mobility, denoted as $\langle \mu_t \rangle = (L/WC_tD_s)(1/V_d)(\partial I_d/V_g)$, where C_t is the capacitance

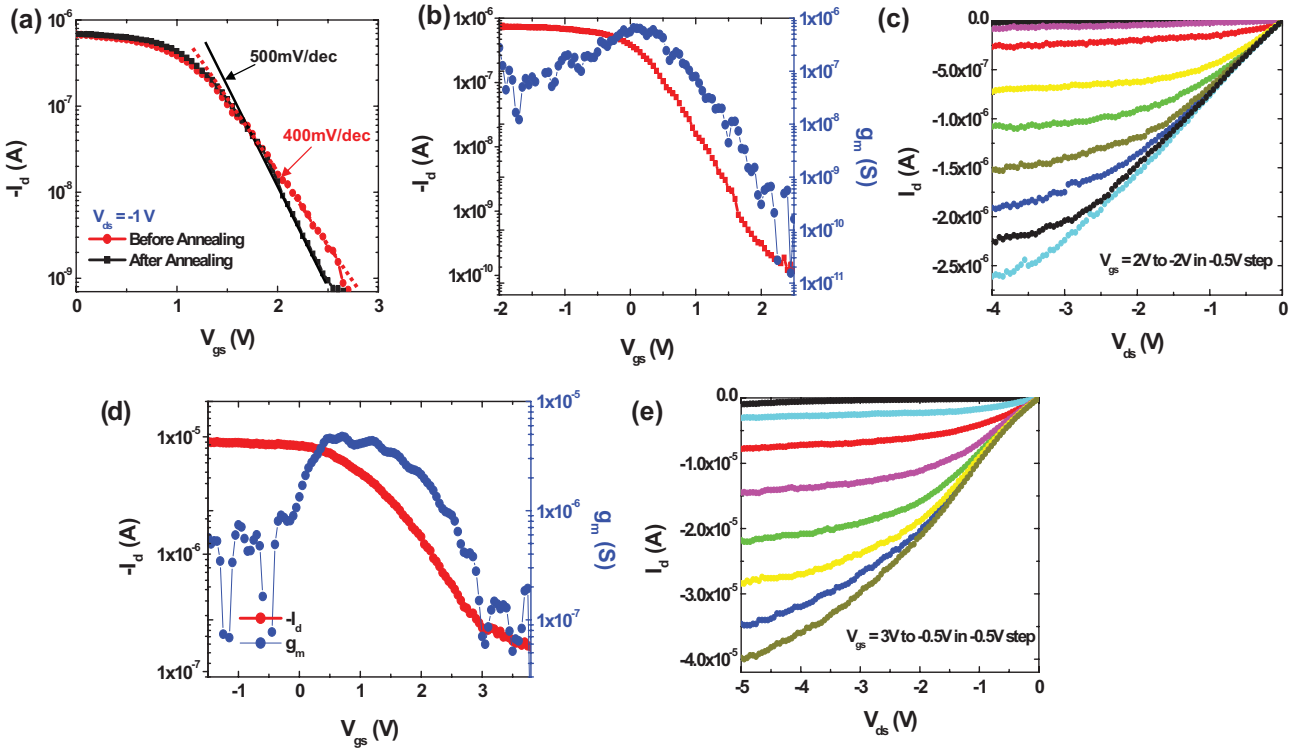

Figure 3. Measured characteristics of depletion-mode p-type SWNT-TFTs with gate length of 2 μm, fabricated using the electrical burning procedure, showing a representative device with 6 μm width (a–c) and another with 50 μm width (d–e), all following annealing unless indicated. a) Drain current vs gate-source voltage at $V_{ds} = -1$ V for a device prior to annealing (red) and after annealing (black). b) Drain current and transconductance versus gate-source voltage at $V_{ds} = -1$ V. c) Drain current versus drain bias as a function of gate bias. d) Drain current and transconductance at $V_{ds} = -1$ V versus gate-source voltage. e) Drain current versus drain bias as a function of gate bias.

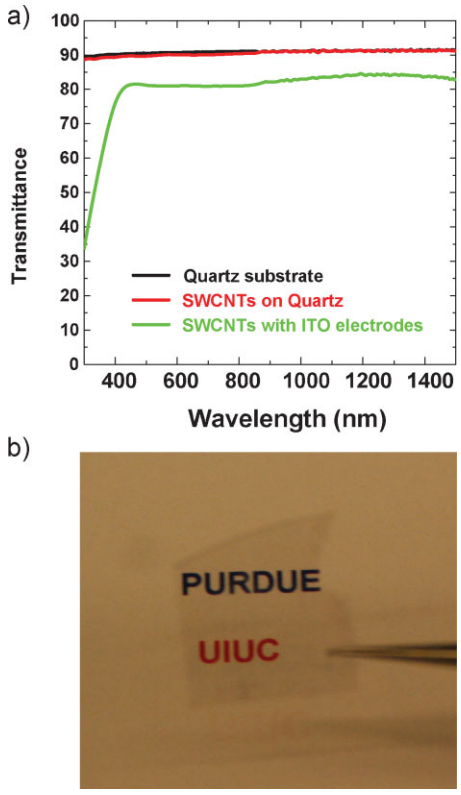

Figure 4. a) Optical transmission spectra as a function of wavelength through quartz substrates i) before and ii) after deposition of SWNT arrays and iii) after TFT fabrication. b) Photograph of a quartz substrate containing fully transparent SWNT-TFTs held over a sheet of paper containing printed text.

per unit length for a semiconducting tube in the array, L is the channel length, W is the physical width of the source/drain electrodes, and D_s is the density of semiconducting nanotubes spanning the channel.[8,10] The aligned-array SWNT-TFTs with 50 μm source/drain width show a maximum transconductance ($g_m = dI_d/dV_{ds}\big|_{V_{ds}=-1V}$) of 4.78 μS and an extracted mobility of ~756 $cm^2\ V^{-1}\ s^{-1}$. The maximum on-current is ~40 μA at $V_{ds} = -4$V and $V_{gs} = -0.5$ V (Fig. 3e). Compared to Pd source/drain contacts with a Pd work function (Φ_m) of 5.2 eV, ITO source/drain contacts have a slightly lower Φ_m of 4.9 eV,[15] which results in a slightly larger Schottky barrier height for the holes, and a slightly higher contact resistance.

Figure 4a shows the measured optical transmission spectra in the visible range for the quartz substrate, the arrays of SWNTs, and the finished TFTs. The curves have not been corrected for substrate transmission. The measured optical transmissions in the 300–1500 nm wavelength range are ~91% for the quartz substrate and ~90% for the aligned SWNT arrays on the quartz substrate. The 1% difference between the optical transmissions of bare quartz and SWNTs on quartz indicates that the transmission losses of carbon nanotubes are negligible. This is consistent with the expected behavior, given the small spatial coverage within the array due to the small SWNT diameter. The SWNT-TFT array substrate contains 600 transistors within an area of 0.5 cm × 0.5 cm. In these samples, the ITO electrodes cover over 70% of the total area. An optical transmission of ~83% is observed in the device sample. Since the HfO_2 is expected to be relatively transparent, the predominant absorption is thought to be associated with the ITO contacts. When observed under the optical microscope, ITO contacts can be easily distinguished by their slightly darker appearance compared to the rest of the structure. The level of overall transmission is comparable to that observed in prior studies employing transparent contact materials, including transparent nanowire-TFTs (82%)[1] and TFTs based on SWNT networks (80%).[2] Figure 4b shows a photograph of the fully transparent SWNT-TFTs devices held over a sheet of paper; the print on the paper is clearly seen though the transparent SWNT-TFTs. Transistor technologies using well-aligned SWNT-TFTs with ITO gate and source/drain electrodes could overcome limits of poly-silicon and amorphous silicon TFTs, which are difficult to extend to transparent electronics because of non-transparent active materials and metal electrodes. Moreover, transistor characteristics, especially mobility, subthreshold slope, and operating voltage, of well-aligned SWNT-TFTs devices are much better than those of low temperature polycrystalline silicon (LTPS)-TFTs and α-Si-TFTs,[3,4] which result in low power consumption and fast switching properties.

In conclusion, fully transparent SWNT-TFTs with ITO as the source/drain gate electrodes and ALD HfO_2 as the gate insulator are demonstrated. The advanced technique of aligned SWNT arrays improves SWNT integration and transistor characteristics, showing an on-current of ~40 μA and a transconductance of ~4.78 μS. Electrical burning is effective for improving transistor characteristics, especially for providing a high yield of transistors with $I_{on}/I_{off} > 10^3$. The optical transmission of fully transparent SWNT-TFTs is ~83%. Fully transparent SWNT-TFTs will not only improve aperture ratio efficiency in active matrix arrays, but will also realize low-power fully transparent nanoscale electronics. These results suggest new opportunities for manufacturing transparent circuits using transparent SWNT-TFTs with ITO contacts.

Experimental

Synthesis of Aligned SWNT Arrays and Electrical Burning: A quartz substrate is thermally annealed at 900 °C in air for 8 h. After thermal annealing, the substrate is cooled slowly (5 °C min^{-1}) to avoid cracking. Catalysts are patterned by UV photolithography (Shipley 1813). 2~5 Å thick catalysts are formed by the electron beam deposition of iron (3×10^{-6} torr; Temsescal CV-8) followed by a lift-off process using acetone. Heating to 900° C in hydrogen ambient conditions (150 sccm) activates the catalyst. A flow of CH_4 and H_2 at 150 sccm at 900 °C for 30 min yields the aligned SWNT array on the quartz substrate. Electrical burning of metallic nanotubes is performed in air using a semiconductor parameter analyzer (HP 4156A). The sweeping speed of the drain bias up to 20 V is defined by long time scan (an instrument setting).

Instrumentation: The transmission spectra of normal incident linearly polarized light is collected using a Lambda 950 spectrophotometer from Perkin-Elmer. Electrical characterizations are done using a semiconductor parameter analyzer (HP 4156A).

Uncited References: [16]

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