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DC modeling and the source of flicker noise in passivated carbon nanotube transistors

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Abstract

DC and intrinsic low-frequency noise properties of p-channel depletion-mode carbon nanotube field effect transistors (CNT-FETs) are investigated. To characterize the intrinsic noise properties, a thin atomic layer deposited (ALD) HfO_2 gate dielectric is used as a passivation layer to isolate CNT-FETs from environmental factors. The ALD HfO_2 gate dielectric in these high-performance top-gated devices is instrumental in attaining hysteresis-free current–voltage characteristics and minimizes low-frequency noise. Under small drain–source voltage, the carriers in the CNT channel are modulated by the gate electrode and the intrinsic $1/f$ noise is found to be correlated with charge trapping/detrapping from the oxide substrate as expected. When thermionic emission is the dominant carrier transport mechanism in CNT-FETs under large drain–source voltages, the excess $1/f$ noise is attributed to the noise stemming from metal–CNT Schottky barrier contacts as revealed by the measurements.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Carbon nanotubes (CNTs) represent an important class of nanoscale building blocks for future beyond-CMOS electronics. Low-power field effect transistors (FETs) based on CNTs have recently achieved close to ideal subthreshold swing and near ballistic transport [1, 2]. Major challenges in implementing electronic systems based on CNT-FETs are device yield, reproducibility and performance uniformity, which depend upon various parameters including nanotube diameter, chirality, contact resistance and gate oxide nanotube interface quality [3–5]. However, relationships between reliability, quality of CNT-FETs and above listed parameters have not been established due to lack of reproducible devices. Quality and reliability of various semiconductor devices are correlated to their low-frequency noise [6–8]. Such studies have not been carried out on CNT-FETs. These observations point to a need for more parametric studies correlating device reproducibility, quality and reliability with low-frequency noise.

In-depth low-frequency noise studies of CNT transistors and resistors can identify high contact resistance and device imperfections such as charge trapping centers along the nanotube as well as its interface with gate oxide. Unpassivated back-gated nanotube transistors and resistors reported in the literature have exhibited high low-frequency noise characteristics [9–11]. This is mainly due to the fact that the nanotube–oxide interface in these devices is exposed to various environmental factors, such as water molecule [12], mobile ions [13], and carrier traps in the oxide [14]. The $1/f$ noise characteristics in such devices are determined by extrinsic factors arising from ambient conditions rather than by intrinsic properties of the nanotube or the necessary interfaces (i.e. nanotube–oxide interface and Schottky barrier contacts). Such noise studies cannot be used to understand the inherent noise characteristics of CNT-FETs. Additionally,

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large amplitudes of low-frequency noise increase the minimum detectable signal at low frequencies and have an adverse effect on nonlinear circuits implemented using CNTs through noise up-conversion. A high quality passivation layer on CNT-FET not only improves the minimum detectable signal but also allows the device to be isolated from its environment. The latter results in stable DC characteristics and reduced low-frequency noise suitable for device quality and reliability studies.

In this paper, we report nearly hysteresis-free current–voltage (IV) characteristics and low low-frequency noise of a top-gated depletion-mode p-channel CNT-FET that have been passivated using a high quality atomic layer deposited (ALD) HfO_2 gate oxide. The measured $1/f$ noise of the device stems from either the excess noise in the Schottky barrier contacts or charge trapping–detrapping at CNT/oxide interface. Based on these results, a model for low-frequency noise in CNT-FETs is proposed and dominant mechanisms responsible for $1/f$ noise in various device operation modes are discussed.

2. Implementation of top-gated CNT-FETs and current–voltage model

The CNT-FET device studied here is shown schematically in figure 1(a) and is fabricated on a high resistivity Si substrate ($\rho \sim 10$ kΩ) covered with a 300 nm SiO_2 thermal oxide. Fe catalyst patterns are defined by UV photolithography with a 10 μm spacing and subsequent Fe deposition and lift-off. CNTs are then synthesized by chemical vapor deposition (CVD) using CH4 as the carbon source on the substrate coated with patterned Fe catalyst. Pd source/drain electrodes are fabricated by lift-off and lithographically defined with a spacing of 3 μm. A 20 nm high-k HfO_2 film is deposited using ASM Micro-chemistry F-120 ALCVD^{TM} Reactor at 300 °C by using precursor of $HfCl_4$ and H_2O. $HfCl_4$ and water (H_2O) are used as precursors for HfO_2 film growth. The pulse length and N_2 purge time are 0.8 and 2.0 s for $HfCl_4$, and 1.0 and 2.0 s for H_2O, respectively. The nucleation of ALD is extremely important for continuous and pinhole-free ultrathin films. If the ALD precursors do not effectively react with the initial substrate, then the ALD film may not nucleate at all or may nucleate only at particular defect sites on the initial substrate. Using DNA functionalization [15] of carbon nanotubes instead of ordinary ALD greatly increases the nucleation sites on the surface due to alteration of the surface chemistry. The surface of the CNT is very inert (due to lack of dangling bonds) and does not contain chemical species that allow for the reaction of either $HfCl_4$ or H_2O during ALD process. As a result, nucleation of gate dielectric film growth by ALD cannot be initiated directly on the surface of CNTs. Instead, the ALD nucleation and growth takes place on the surrounding quartz (SiO_2) support substrate which results in the eventual drowning of CNTs by gate dielectric as the film thickness increases beyond the nanotube diameter (>5 nm for conformal coating).

Top gate metal is defined by UV photolithography followed by the deposition of Cr/Au (10/50 nm) with a minimum gate length of 1.5 μm. Cr/Au (20/450 nm) metal interconnects are finally deposited on top of the source and drain. In order to study the inherent properties of a single nanotube in a controlled environment, an attempt was made to obtain only one semiconducting nanotube per device. This was achieved by reducing the nanotube density through adjusting the synthesis condition in order to reduce the chance of having several nanotubes (metallic or semiconducting) in one device. The synthesis process, therefore, resulted in very low yield for devices with one semiconducting nanotube. Figure 1(b) shows a top gate transistor structure with one CNT connecting the source and drain contacts studied in this work.

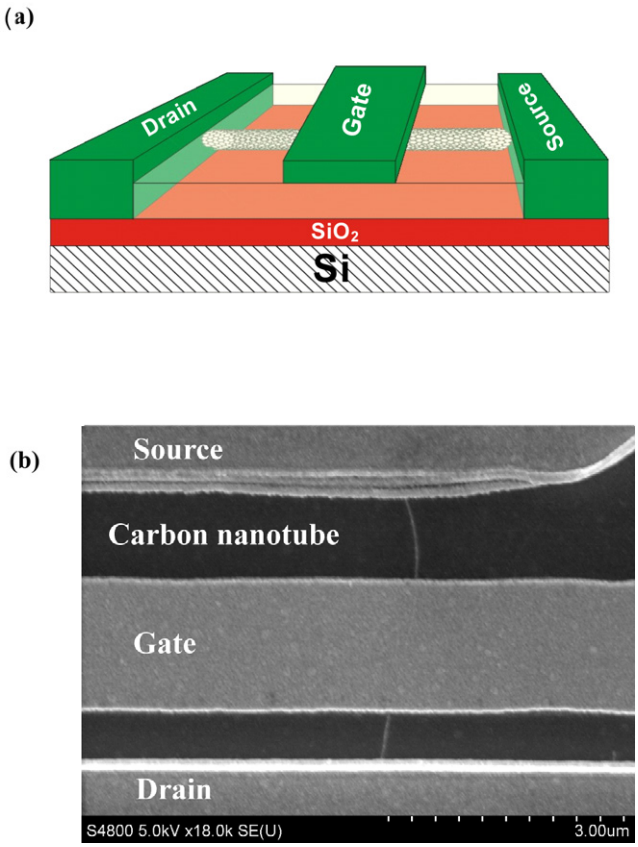

Figure 1. (a) The schematic view of the top gate CNT-FETs with 20 nm thick ALD-grown HfO_2 as gate dielectrics. (b) The SEM image of a device with a single nanotube covered by ALD HfO_2.

Referring to energy-band diagram in figures 2(a) and (b), one can roughly categorizes the mechanism of carrier transport of the top gate transistor as a function of biasing condition into two regimes [16].

(1) Schottky barrier modulation regime: in this regime carriers are controlled by the Schottky barriers between drain/CNT and source/CNT contacts. As the drain bias (V_{sd}) is increased, the Schottky barriers become thinner and help carriers move into the channel by thermionic emission process.
(2) Gate modulation regime: under small drain/source bias ($V_{sd} < 1$ V for device geometries used in this work), the depletion regions of the CNT due to Schottky barriers are short. Carriers that pass from contacts to the channel by thermionic emission are well-controlled by the height of the energy-band and are thus controlled by the gate

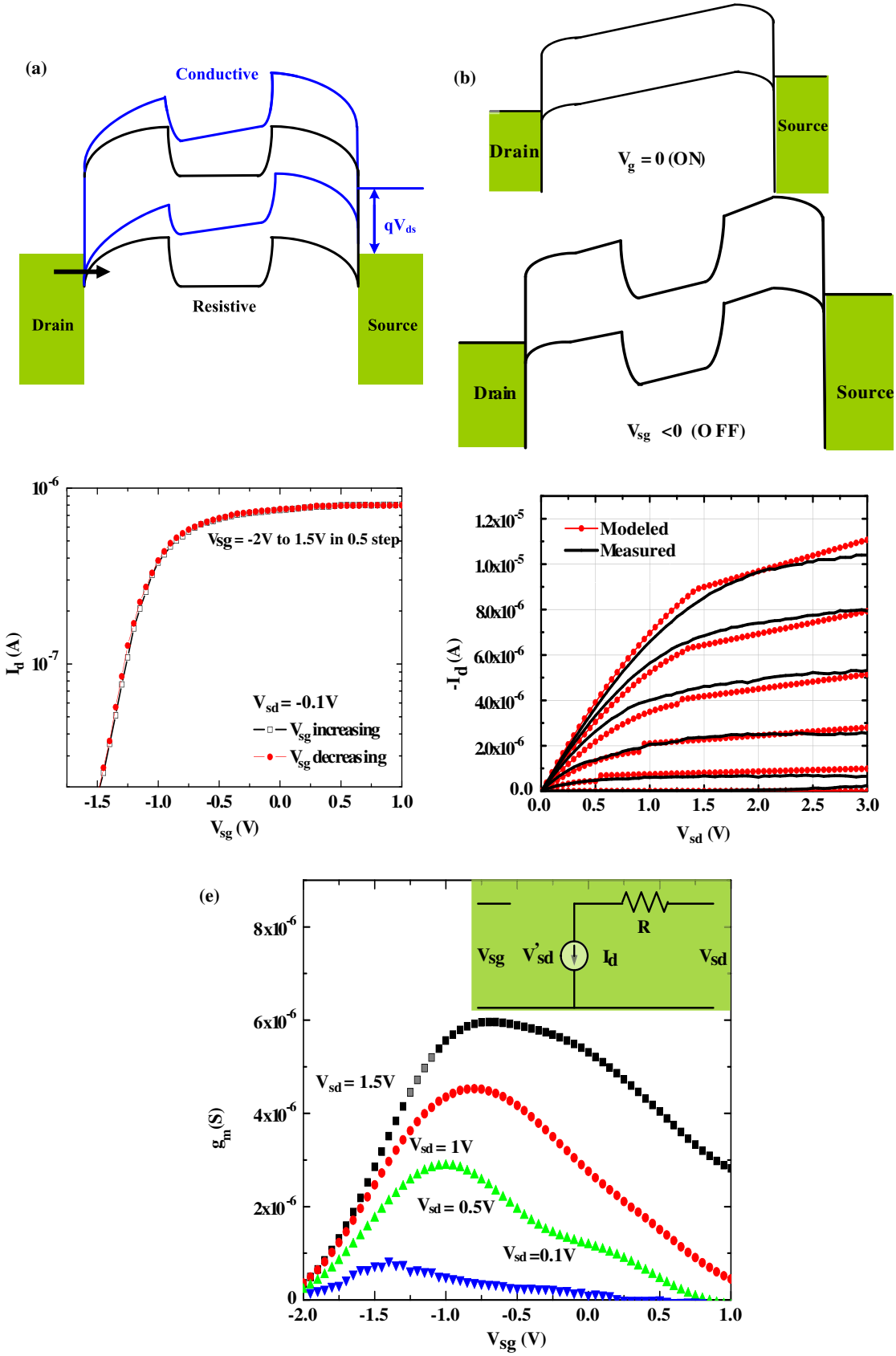

Figure 2. Characteristics and energy-band diagram of a p-type CNT-FETs with HfO_2 as gate dielectrics. (a) Energy-band diagram with source/drain bias at a constant gate bias ($V_{sg} = -1$ V). (b) Energy-band diagrams of a local top-gated CNT-FETs having depletion-mode at ON/OFF state of transistor with gate bias at a constant source/drain bias ($V_{sd} = 1$ V). (c) Current I_d versus V_{sg} as increasing (square) and decreasing gating sweeps (circle). (d) Measured (black) and simulated (red) drain current versus drain bias (V_{sd}–I_d) as a function of gate bias of the same device. The minimum resistance of 120 kΩ is measured. (e) A family of transconductance characteristics plotted as a function of the gate voltage with drain–source voltage as a parameter.

voltage. Long CNT-FETs show gate modulation under a larger drain/source bias V_{sd}.

Figure 2(c) shows transfer characteristics (I_d–V_{sg}) of the CNT-FET with 1.5 μm gate length and 3 μm source–drain separation measured in the ambient environment when V_{sg} is swept from -1.5 to 1 V and back to -1.5 V. Virtually no hysteresis is observed in the IV characteristics of this device. Figure 2(d) shows I_d–V_{sd} characteristics of the same device with a maximum on current of 14 μA derived from one nanotube FET. The extracted small-signal transconductance of the device g_m plotted against gate–source voltage at different drain–source voltages is shown in figure 2(e). A maximum transconductance of 6 μS at a drain bias of $V_{sd} = 1.5$ V and gate bias of $V_{sg} = -0.75$ V is achieved. The inset of figure 2(e) shows a simple equivalent circuit model of the device, where drain resistance (R) due to Schottky barrier at the drain contact connects the intrinsic CNT-FET to the external terminal. Voltage V_{sd} is the external drain bias voltage of the transistor while V'_{sd} is the internal value. Assuming ideal MOSFET charge control equation for simplicity and using the relationship ($V'_{sd} = V_{sd} - R \times I_d$), the I–V characteristics of the CNT-FET in the linear region is given by

$$I_d = \frac{\mu_{eff} C_g}{L}(V_{sg}+V_t)V'_{sd} = \frac{\mu_{eff} C_g}{L}(V_{sg}+V_t)(V_{sd}-RI_d) \quad (1)$$

where L is the gate length, $C_g = 2\pi\varepsilon_0\varepsilon/\cosh^{-1}(1+h/r) \sim 28$ aF nm^{-1} estimated for a cylindrical tube model is the gate capacitance per unit length, $\varepsilon_r = 15$ is the effective dielectric constant of HfO_2, $r = 0.5$–2 nm is the radius of CNT, $h = 20$ nm is the gate oxide thickness and μ_{eff} is the effective field effect mobility of CNT-FETs calculated from $\frac{\partial I_d}{\partial V_{sg}} \times \frac{L}{C_g} \times \frac{1}{V_{sd}}$. Solving for drain current I_d and transconductance g_m in linear region yields:

$$I_d = \frac{\mu_{eff} C_g (V_{sg}+V_t)V_{sd}}{L + R\mu_{eff} C_g (V_{sg}+V_t)},$$
$$g_m = \frac{\partial I_d}{\partial V_{sg}} = \frac{\mu_{eff} L C_g V_{sd}}{[L + R\mu_{eff} C_g (V_{sg}+V_t)]^2}. \quad (2)$$

Drain series resistance R which is the sum of channel resistance R_{ch} and Schottky barriers contact resistance R_{ds} can be directly measured at small V_{sd} where current is roughly $\mu_{eff} C_g (V_{sg}+V_t)V_{sd}/L$.

$$R = R_{ch} + R_{sd} = R_{ch} + R_{d0}\exp(-qV_{sd}/kT). \quad (3)$$

The current in the linear regime can be written as

$$I_d = \frac{\mu_{eff} C_g (V_{sg}+V_t)V_{sd}}{L + \mu_{eff} C_g (R_{ch} + R_{d0}\exp(-qV_{sd}/kT))(V_{sg}+V_t)}. \quad (4)$$

From the IV curves shown in figure 2(d) and assuming a negligible channel resistance R_{ch}, one can extract a zero volt drain resistance R_{d0} of 120 kΩ. The threshold voltage (V_t) of +2 V is also extracted from the measured IV curves. In the current saturation regime when $V_{sd} \geqslant V_{sg} + V_t + RI_d$, CNT-FET has a semi-ballistic transport. Its IV curves can be empirically modeled according to

$$I_d = \frac{K}{2}(V_{sg}+V_{th})^{3/2}(1+\lambda V_{sd}),$$
$$g_m = \frac{\partial I_d}{\partial V_{sg}} = \frac{3K}{4}(V_{sg}+V_t)^{1/2}(1+\lambda V_{sd}) \quad (5)$$

where effective transconductance $K = 3.5 \times 10^{-6}$ (A/V$^{1.5}$), and channel length modulation parameter $\lambda = 0.2$ V^{-1} are estimated from the measured data. Note that the channel resistance does not influence the current in this regime, but limits the semi-ballistic transport current saturation regime to large source–drain voltages V_{sd} and small source–gate voltages V_{sg}. As shown in figure 2(d), a good agreement between the CNT-FET model (equations (4), and (5)) and measured data is achieved.

3. Hysteresis and noise analysis

As reported in the literature [2, 9–11], unpassivated CNT transistors show high amplitudes of low-frequency noise. The extra noise is attributed to charge trapping on or near CNTs caused by carrier injection into and from traps activated by water molecules [5], mobile ions [12], and silicon dioxide [13]. These charge traps change the effective gate potential by modifying the threshold voltage of the transistor and are also responsible for large hysteresis in the IV characteristics of unpassivated CNT-FETs. Figure 3 shows the IV characteristics of a bottom gated CNT-FET with a single unpassivated nanotube having a diameter of $\sim$2 nm. Figure 3(a) shows the hysteresis in the transfer characteristic (I_d–V_{sg}) with respect to various sweeping rates of V_{sg}. A significant dependence of the hysteresis on the V_{sg} scan speed is observed, with slower V_{sg} scan producing larger hysteresis, suggesting that hysteresis is mainly caused by slow trapping and detrapping of carriers (holes) at timescales of the order of a few seconds. Figure 3(b) shows that the amplitude of the gate voltage V_{sg} sweep directly affects the width of the shift in the threshold voltage (hysteresis) indicating that the gate bias induces charge trapping. When drain voltage is swept at a fixed gate voltage, no hysteresis with respect to V_{sd} is observed, indicating that the charge traps are not influenced by the drain voltage and thus the drain region.

Implementation of top-gated CNT-FETs with a high quality gate oxide isolates the device from its environment resulting in nearly hysteresis-free DC characteristics as shown in figure 2(c). These passivated CNT-FETs also allow measurements that can identify the origin of flicker noise in these devices. Here, low-frequency current noise spectra are obtained with a Stanford Research System SR 570 amplifier and a HP 3516A dynamic signal analyzer [17]. All measurements are carried out at room temperature in noise shielding chamber. There are mainly two major sources for flicker noise in these devices, (i) the excess noise in Pd–CNT Schottky barrier leading to generation–recombination noise in the space-charge region including metal–CNT interface, (ii) charge trapping–detrapping phenomena at the CNT/oxide interface.

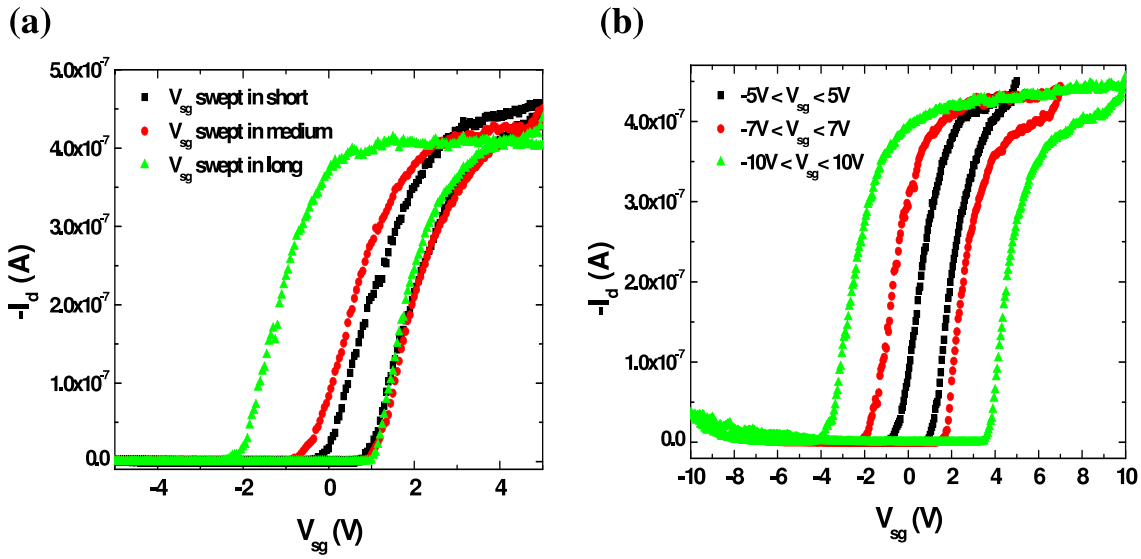

Figure 3. Hysteresis behaviors of I_d–V_{sg} curves for CNT-FETs under different biasing conditions (a) sweeping speeds of gate bias: (squares) fast sweeping rate (circles) medium sweeping rate. (Triangles) Slow sweeping rate with integration of long time. The short, medium, and long term sweeping speeds are default set values of HP 4516, semiconductor analyzer. (b) I_d–V_{sg} curves for CNT-FETs under different ranges of gate bias. Drain bias is applied to 100 mV. At gate bias from 5 to −5 V, a shift of threshold voltage (V_t) is observed in 2 V (squares). At gate bias from 7 to −7 V, a shift of threshold voltage (V_t) is measured in 3.5 V (circles). At gate bias from 10 to −10 V, a shift of threshold voltage (V_t) is measured in 7 V (triangles).

We first examine the generation–recombination (g–r) noise in the space-charge region. Kleinpenning [18] has developed a model for g–r noise in the Schottky barrier region. This model assumes that the noise is related to the fluctuations of the barrier height, mobility and diffusion constant in the Schottky barrier region. The current noise is found to be a quadratic function of the Schottky barrier current where carriers are mainly controlled by the barrier. Figure 4(a) shows the dependence of the current noise spectrum (S_I) at 100 Hz and the square of the saturation drain current (I_d^2) versus source–drain voltage V_{sd} ranging from 0 to 2.5 V and at a constant gate bias V_{sg} of 1 V. The current noise S_I is proportional to the squared drain current (I_d^2) over most of the applied drain bias. Charge trapping in the space-charge region and the interface charges between CNT and Pd electrodes lead to generation-recombination of carriers and thus fluctuation in the current flowing in the channel similar to the current noise of Schottky diodes [19, 20]. Previously, we have reported polymer electrolyte-gated CNT-FETs with similar trend observed for the current noise (S_I proportional to I_d^2) [19]. In polymer electrolyte-gated CNT-FETs transport mechanism of holes is also governed by the Schottky barrier as the polymer gate overlaps with source and drain contact areas. Thermionic emission of holes across the Schottky barrier is the dominant transport mechanism in the active transistor operation mode.

Figure 4(b) shows the measured $1/f$ noise of the charge trapping–detrapping phenomena between the oxide and a CNT with diameter of 2 nm, when drain voltage V_{sd} is fixed at 0.2 V. Under a small drain bias, the Schottky barriers do not influence the transport and carriers are modulated by local gate-biasing similar to a MOSFET in linear/triode regime. Current fluctuation in this mode of operation is due to trapping/detrapping processes involving interface traps and trapped charges in the oxide layer. Based on the measured $1/f$ noise one can construct a noise model as the following. According to Hooge's empirical law, the $1/f$ current noise amplitude can be written as

$$\frac{S_I(f)}{I_d^2} = \frac{\alpha_H}{fN} \tag{6}$$

where α_H is the Hooge's constant and $N = C_g L(V_{sg} + V_{th})/q$ is the total number of carriers in CNT-FET channel. In the linear region, equations (2) and (6) can be combined to yield

$$S_I(f) = \frac{\alpha_H q \mu_{eff}}{fL^2} V_{sd} g_m (V_{sg} + V_t). \tag{7}$$

For a small constant source/drain voltage, the current noise amplitude is proportional to $g_m(V_{sg} + V_t)$ as shown in figure 4(b).

In the saturation regime, using equations (5) and (6), we can find the amplitude of current noise as

$$S_I = \frac{4q\alpha_H (g_m)^2}{9fC_g L} \frac{V_{sg} + V_{tp}}{1 + \lambda V_{sd}}. \tag{8}$$

This type of low-frequency noise is often masked by the Schottky barrier noise that dominates the noise characteristics of CNT-FETs under large source/drain bias voltage V_{sd}.

Once the environmental effects contributing to excess noise are suppressed in passivated CNT-FETs with ALD HfO_2 gate oxide, one can observe two different regimes of operation. Due to the noisy nature of Schottky contacts to CNT, the amplitude of noise (S_I) at 100 Hz is proportional to the square of drain current at large source/drain bias voltages of $V_{sd} >$ 1 V. For small drain voltage of $V_{sd} = 0.2$ V, the amplitude of current noise (S_I) at 100 Hz is closely correlated to the

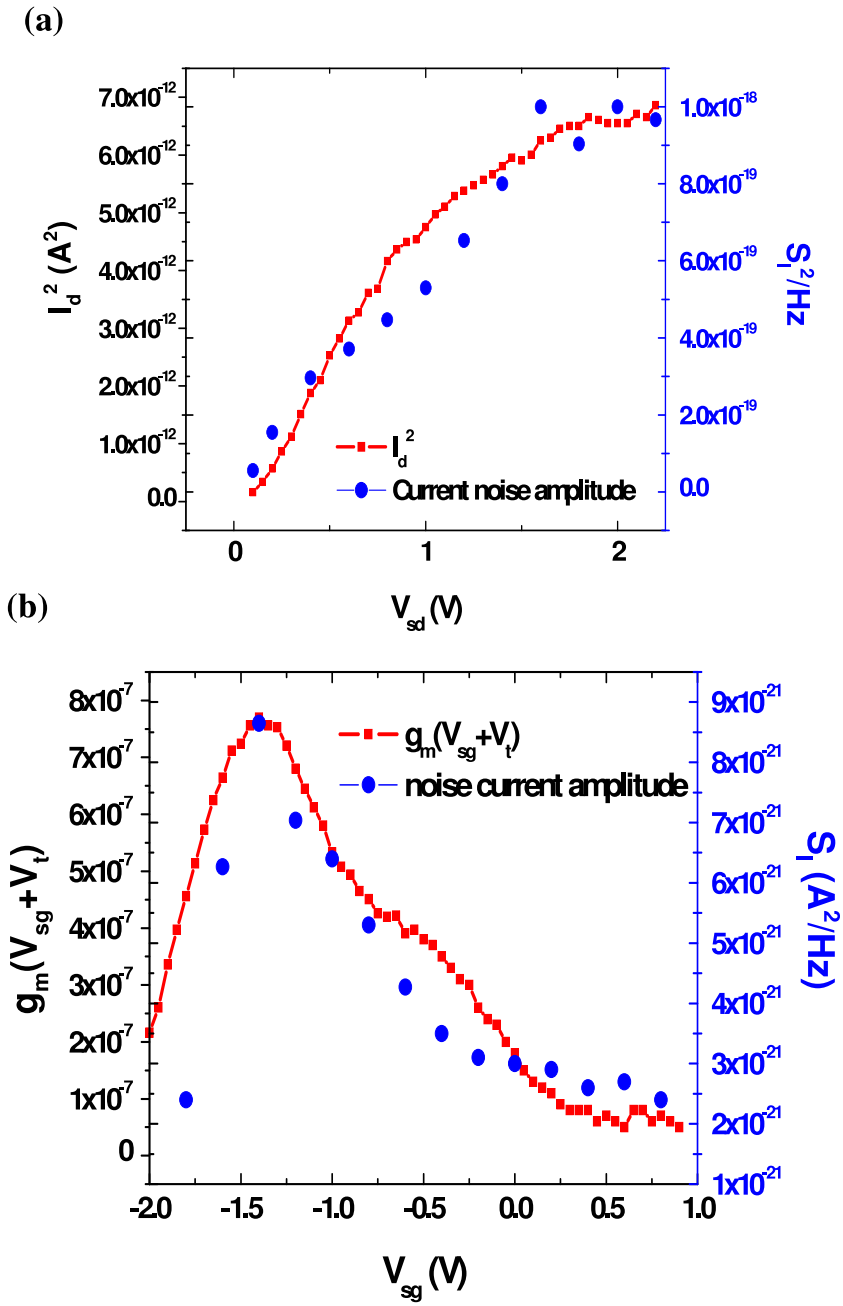

Figure 4. (a) Measured I_d^2 and the amplitude of current noise spectrum (S_I) at 100 Hz plotted as a function of drain bias at constant gate bias of 1 V. (b) The transconductance versus the amplitude of current noise (S_I) with a function of V_{sg} at the drain voltage of 0.2 V. Current noise amplitude at different drain bias can be expressed as a function of g_m.

gate transconductance multiplied by the effective gate voltage. While the noise study is performed on only one CNT-FET device passivated with ALD HfO_2 gate oxide, other top-gated CNT-FETs fabricated by ALD Al_2O_3 and ZrO_2 gate oxide have been reported by our group and confirm the noise measurement trends observed here [16, 21]. Under small drain bias, current fluctuations in these devices are due to trapping/detrapping process involving interface traps and trapped charges in the oxide layer, resulting in the intrinsic $1/f$ noise correlation with device transconductance. At high drain bias the current noise is not proportional to I_d^2 as the Schottky barrier does not influence the transport of carriers in these devices [19].

4. Conclusion

We have demonstrated that the $1/f$ noise of a high-performance depletion-mode CNT-FET with ALD HfO_2 gate oxide originates from the superposition of excess noise in metal–CNT Schottky barrier and charge trapping–detrapping phenomena between oxide and CNT. Under small drain/source voltages in the linear regime of operation, the $1/f$ noise of CNT-FETs, mainly affected by the gate bias, is dominated by charge trapping–detrapping phenomena. On the other hand, as carriers transport is controlled by the Schottky barrier under large source/drain voltage, the $1/f$ noise is proportional to

the square of drain current (I_d^2) similar to Schottky barrier diodes. The ALD HfO_2 passivation layer on CNT helps in lowering the $1/f$ noise of CNT-FET from the interaction with ambient environment, allowing intrinsic current fluctuations to be examined in top-gated CNT-FETs.

Acknowledgments

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