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Current on/off ratio enhancement through the electrical burning process in ambient with/without oxygen for the generation of high-performance aligned single-walled carbon nanotube field effect transistors

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We present characteristics of the electrical burning process with/without oxygen-ambient for parallel aligned single-walled carbon nanotube field effect transistors (SWNT-FETs). High selectivity of metallic and semiconducting nanotubes is demonstrated by an electrical burning process through partial etching of the atomic layer deposited Al_2O_3 layer beneath the gate electrodes. Metallic nanotubes exposed to oxygen show electrical breakdown during the burning process, resulting in the SWNT-FETs having excellent performance. Specifically, 100 μm source/drain width p-type aligned SWNT-FETs through electrical burning with local oxidation show high I_{on}/I_{off} ratios ($>10^3$), 10 μS at a drain bias of -1 V and -100 μA at a reverse gate bias of -8 V. © *2010 American Institute of Physics*. [doi:10.1063/1.3504689]

Single-walled carbon nanotube field effect transistors (SWNT-FETs) have been the focal point of the research on devices for electronic circuit applications and integrated sensors, due to their excellent electrical properties (e.g., ballistic transport and high current capability), which originate from their one-dimensional nanostructure.[1–4] For the implementation of large integrated circuits and high performance devices, advanced growth techniques and fabrication methods have been studied intensively with a view toward producing Si complimentary metal-oxide-semiconductors.[3–5] The recent literatures have proved the basic concepts to realize a simple integration,[3] such as a single transistor,[6] logic circuits,[7] and a ring oscillator[8] utilizing SWNTs as the channel. Among these techniques, a innovative approach[3–5] in realization of complex circuits and high-performance devices was proposed in which perfectly aligned arrays of SWNT on a miscut quartz wafer were used to create SWNT-FETs with a top-gated structure, leading to atomic step-templated growth of the aligned SWNTs. The top-gated aligned array SWNTs show a high integration to synthesize them selectively, and excellent electrical properties for high-performance devices when coupled with atomic layer deposited (ALD) gate oxide or epoxy (SU-8).

In order to improve I_{on}/I_{off} for the top-gated aligned SWNTs transistor, an electrical burning process[3,4,9] (a self-heating due to application of a drain/source bias in air) is utilized to remove metallic nanotubes selectively. However, these techniques, based on only two terminals (i.e., source and drain), are limited in terms of their ability to monitor and prove the improvement of I_{on}/I_{off} for transistors in real time, unlike three-terminal devices. On the other hand, the ALD or epoxy gate insulator of the three-terminal device prevents oxygen in the ambient from reaching SWNTs[4,6] during the electrical burning process. As a result, it is difficult to oxidize the metallic SWNTs during the process, resulting in the survival of numerous metallic nanotubes. Nevertheless, there is no report to date which focuses on the difference in the oxidizing effect when the electrical burning process is executed using the top-gate of the aligned SWNT-FETs.

We report that an electrical burning, based on a local oxidation, in aligned SWNT array FETs can afford a high yield retaining high I_{on}/I_{off} for a transistor, as compared to the previous two-terminal electrical burning methods swept by only source-drain voltage. In order to demonstrate electrical burning from local oxidation, we build two different structures of parallel aligned SWNT array FETs on quartz substrates. One (reference) has an ALD Al_2O_3 layer covering the entire SWNT region, such that oxygen-ambient is blocked by the insulator. On the other hand, the ALD Al_2O_3 layer (local oxidation) remains only beneath the top-gate region, which is achieved using a partial etching technique. Electrical burning is performed via self heating by sweeping a high drain/source bias at a gate bias which results in a semiconducting nanotube off-state. Then, a comparison of I_d-V_{gs} curves in the two different devices is performed. Here, the comparison demonstrates that the local oxidation helps to remove metallic nanotubes in air, and high electrical performance of aligned SWNT-FETs after removing metallic SWNTs is observed.

For the generation of the parallel aligned SWNT-FETs with a top-gate on a quartz substrate, the fabrication process is as follows: prior to the growth of the SWNTs, a ST-cut quartz substrate is annealed for 8 h at 900 °C in air. Catalysts, 2–5 Å thick, patterned by a photo process (Shipley 1805 photoresist), are deposited by electron beam deposition of iron ($\sim 10^{-5}$ torr;Temescal CV-8). The synthesis of the carbon nanotubes in a chemical vapor deposition (CVD) chamber consisted of two steps, a surface pretreatment step and a growth step. The iron catalysts are calcinated in air for ~30 min at 500 °C, and the temperature is ramped up to 900 °C during surface pretreatment ($Ar:H_2 = 80\%:20\%$). Hydrogen promotes rapid dewetting of the nanoporous film, leading to a dispersed array of discrete catalyst nanoparticles.

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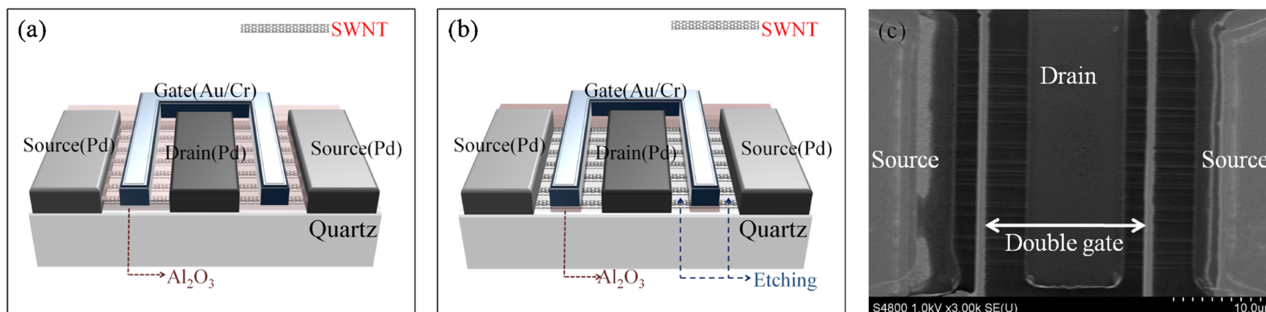

FIG. 1. (Color online) Schematic views of the top-gate aligned array of SWNT-FETs with a 30-nm-thick Al_2O_3 gate insulator: (a) the insulator is covered on the entire SWNTs regions and in the case of (b) the insulator is only beneath the gate region. (c) SEM image of an aligned array of SWNT-FETs, corresponding to (b).

The synthesis of the aligned SWNT array is performed using a flow of H_2/CH_4. The grown carbon nanotubes had a diameter of 1–5 nm, with a tube density of four SWNTs/micrometer. The ALD Al_2O_3 film is subsequently deposited on the aligned array of SWNTs, utilizing an ASM Microchemistry F-120 ALCVD™ reactor. A 30 nm amorphous Al_2O_3 film is deposited on the wafer at 300 °C. Using wet etching involving diluted HF solution, the ALD Al_2O_3 oxide corresponding to the source and drain patterns with spacing of 5 μm is removed. Electron beam deposition of Pd is then performed to form source and drain metal contacts in the middle of two catalyst patterns with a spacing of 20 μm. Lastly, gate metals are deposited, i.e., Cr/Au (20/100 nm) with a minimum gate length of 1.5 μm. Figure 1(a) shows the schematic structure of the aligned SWNTs FET fabricated on a quartz wafer. Local oxidation devices are formed by wet etching (diluted HF solution) from Fig. 1(a); thus, ALD oxide beneath the gate metals remains, while the boundary oxide between the source/drain and gate is finally opened by diluted HF solution, as shown in Fig. 1(b). Figures 1(b) and 1(c) are the schematic diagram and scanning electron microscope (SEM) image of the final structure, respectively.

In general, 50% of metallic and 50% of semiconducting carbon nanotubes are randomly grown during the synthesis of SWNTs.[10] As a result, the metallic nanotubes bridged the source and drain, and then degrade I_{on}/I_{off} in parallel aligned SWNT-FETs arrays. In order to enhance I_{on}/I_{off} and maintain a high yield of SWNT-FETs, a simple and reliable electrical burning process should be performed to remove the metallic nanotubes from the parallel arrays entirely. However, Fig. 2(a) shows that the parallel aligned SWNTs having a passivated structure [Fig. 1(a)] would not burn at a drain voltage of up to 40 V, as long as a positive gate voltage of 8 V is applied for ensuring turn-off in the semiconducting nanotubes. In order for doing electrical burning at lower voltage, the structure of the parallel aligned SWNTs is modified through etching the boundary oxide between source/drain and gate by diluted HF solution. As a result, the aligned SWNTs are exposed to air, especially oxygen, with the exception of the region beneath the gate, as shown in Figs. 1(b) and 1(c). Using the structure exposed to oxygen, Figs. 2(b) and 2(c) show current-voltage (I-V) curves measured while executing the electrical burning process, where the positive gate voltage is 8 V, such that the positive gate voltage can turn the semiconducting SWNTs off. The current drop of the

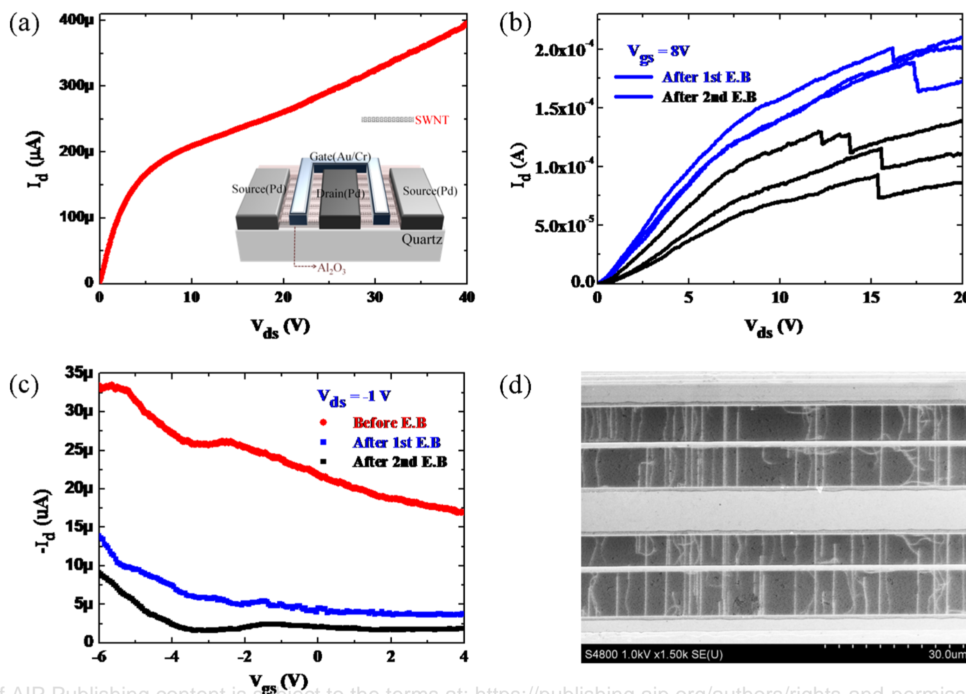

FIG. 2. (Color online) (a) I_d-V_{ds} characteristic of the aligned array of SWNT-FETs having the structure shown in Fig. 1(a): electrical breakdown of SWNTs passivated by ALD Al_2O_3 does not occur up to a drain bias of 40 V. (b) I_d-V_{ds} characteristic of the aligned array of SWNT-FETs having the structure shown in Fig. 1(b): electrical breakdown occurs around 15 V in air. (c) I_d-V_{gs} characteristic of the aligned array of SWNT-FETs of SWNTs having the structure shown in Fig. 1(b), and measured after electrical breakdown occurs, as described in Fig. 2(b). (d) SEM image of a burnt nanotube after the burning and measurement process.

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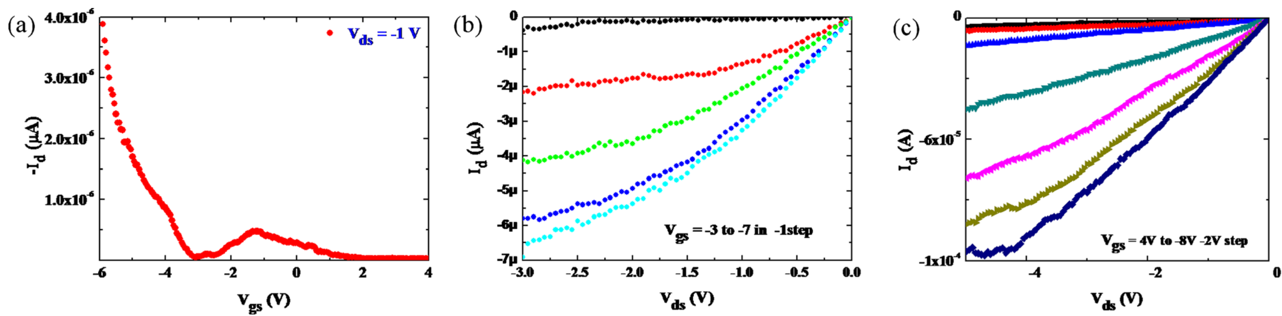

FIG. 3. (Color online) Characteristics of a p-type SWNT-FET with ALD Al_2O_3 and a width of 10 μm [(a) and (b)] and 100 μm (c), after electrical burning. (a) Current I_d vs V_{gs} for a 1.5 μm gate length SWCNT-FET at V_{ds}. (b) Drain current vs drain bias as a function of gate bias. (c) Drain current vs drain bias at a width of 100 μm.

blue and black lines, representing sequential electrical breakdown due to the removal of the metallic SWNTs, are observed at a drain/source bias of around 15 V. The sequential burning process can enhance the I_{on}/I_{off} to 10^3, i.e., at least two orders of magnitude higher than the original device. Figure 2(d) is the SEM image after the electrical burning procedure. Most electrical breakdown of the metallic SWNTs occurred in the region between the source/drain and gate that the oxygen ambient could be reached.

Here, the difference of I_d-V_{ds} between Figs. 2(a) and 2(b) should originate from the local oxidizing effect of metallic SWNTs. In the case of the structure of Fig. 1(b), since the electrical burning process is performed in oxygen ambient while applying a gate voltage of 8 V, the current flows mainly through metallic SWNTs. After reaching the saturation region of the current value by sweeping the drain/source bias, the dissipative electrical power affords self-heating of SWNTs, thus heat energy can activate a local oxidation process between the C–C bonds inside metallic SWNTs and oxygen in the air, resulting in the generation of CO_2 gas and the removal of the SWNTs. On the other hand, in case of the passivated SWNT-FETs, shown in Fig. 1(a), it is difficult to perform the local oxidation process during the electrical burning process, since the ALD Al_2O_3 layer prevents oxygen from reaching the SWNTs;[3] thus, the electrical burning process does not occur until the drain/source bias is at least 40 V. With an activated energy and oxygen ambient, the partial etching technique as shown in Fig. 1(b) can contribute to any gate oxide layer, such as HfO_2, SiO_2, and SiN_x.

Figure 3 shows the transistor characteristics of the aligned SWNTs-FET with a 1.5 μm gate length, SWNT-FET with 30-nm-thick Al_2O_3 and a source/drain width of 10 μm [Figs. 3(a) and 3(b)], 100 μm [Fig. 3(c)] after metallic nanotubes are removed. The maximum intrinsic transconductance, $g_m = dI_{ds}/dV_{ds}|_{V_{ds}=-1\ V}$ of 1.8 μS, and a field effect mobility of $\sim$610 $cm^2\ V^{-1}\ S^{-1}$ are obtained. The device shows a maximum on-current of -7 μA at $V_{ds}=-3$ V and $V_{gs}=-7$ V. Figure 3(c) shows the I_d-V_{gs} characteristics of an aligned SWNT-FET with a width of 100 μm. Following the electrical burning, the channel contains approximately 15 aligned SWNTs. A recent report[4] shows the average per tube mobility, denoted as $\langle \mu t \rangle = (L/WC_tD_s)(1/V_d) \times (\partial I_{ds}/V_g)$, where C_t is the capacitance per unit length for a semiconducting tube in the array, L is a gate length, and D_s is the density of the semiconducting nanotube spanning the channel. The field effect mobility of an aligned array of SWNT-FETs with 100 μm source/drain width was found to be 2890 $cm^2\ V^{-1}\ S^{-1}$. The maximum on-current is ~ -100 μA at $V_{ds}=-4$ V and $V_{gs}=-8$ V, as shown in Fig. 3(c).

In conclusion, we fabricate SWNT-FETs in a 1.5 μm gate length with a 30 nm thick ALD with/without an opening window allowing oxygen to reach SWNT-FETs. Using these structures, the electrical burning process with/without an oxygen-ambient is evaluated in terms of monitoring and improving I_{on}/I_{off} for transistors in real time. After the electrical burning process is performed, I_{on}/I_{off} for the transistor increased by two orders relative to the original device, and the maximum intrinsic transconductance $=1.8$ μS, the field effect mobility $\sim$610 $cm^2\ V^{-1}\ S^{-1}$, the maximum on-current ~ -7 μA at $V_{ds}=-3$ V, and $V_{gs}=-7$ V is achieved when three semiconducting SWNTs with 10 μm source/drain width are used for the measurement. Furthermore, the field effect mobility and the maximum on-current of the aligned array of the SWNT-FETs 100 μm source/drain width are 2890 $cm^2\ V^{-1}\ S^{-1}$ and ~ -100 μA at $V_{ds}=-4$ V and $V_{gs}=-8$ V, respectively. These results suggest opportunities for manufacturing integrated circuits using aligned single-walled nanotubes arrays with high yield.

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