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Atomic-layer-deposited ZnO thin-film transistors with various gate dielectrics

Jaehyun Yang[1], Joong Keun Park[1], Sunkook Kim[2], Woong Choi[3], Sangyoon Lee[4], and Hyoungsub Kim[*,1]

[1] School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon 440-746, Korea
[2] College of Electronics and Information, Institute for Laser Engineering, Kyung Hee University, Yongin 446-701, Korea
[3] School of Advanced Materials Engineering, Kookmin University, Seoul 136-702, Korea
[4] Samsung Advanced Institute of Technology, Yongin 446-712, Korea

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[*] Corresponding author: e-mail hsubkim@skku.edu, Phone: +82 31 290 7363, Fax: +82 31 290 7371

We have investigated the effects of gate dielectric layers having different microstructures on the crystallographic properties and device performances of atomic-layer-deposited (ALD) ZnO thin-film transistors (TFTs) in a bottom-gated structure. Among three gate dielectric materials (thermally grown SiO_2, ALD-HfO_2, and ALD-Al_2O_3), the ALD-ZnO layer on Al_2O_3 exhibited the best crystallinity and surface morphology due to the excellent surface roughness and/or hydrophilic surface polarity of the amorphous Al_2O_3 layer. As a result, it showed the best TFT performance, including field-effect mobility (~3.9 cm^2/Vs), subthreshold swing (~1.35 V/decade), and on/off ratio (~5×10^7).

1 Introduction There has been a continuous pursuit of high-performance thin-film transistors (TFTs) that have low-temperature process capability to realize mechanically flexible and/or optically transparent displays [1]. ZnO-based TFTs are particularly attractive since they can provide relatively high mobility, low temperature processing, compatibility with flexible substrates, and optical transparency [2]. Among several deposition methods for ZnO thin films, growing interest has been given to an atomic layer deposition (ALD) technique, as it allows high-precision thickness control, high uniformity to achieve large-area deposition, and low defect density [3].

In addition to the study of metal-oxide-based channel layer itself, lots of studies have focused on high-k films synthesized via either ALD or other techniques, which could be used as gate dielectric materials to improve TFT performance [4–10]. When ALD-ZnO is used as a channel layer in a bottom-gated TFT structure, the identity of the underlying gate dielectric is extremely important, because the ALD process is strongly dependent on the starting surface condition due to its surface-saturation controlled deposition kinetics [11]. Meanwhile, a single-layered ALD-high-k gate dielectric film may not be well-suited for commercial TFT technology, because it requires a long process time to reach a thickness that can allow a sufficiently low gate leakage current ($<10^{-12}$ A) in a bottom-gated TFT structure.

In this study, we investigated the effect of different gate dielectric materials – thermally grown SiO_2, ALD-Al_2O_3, and ALD-HfO_2 films – on bottom-gated ALD-ZnO TFT performance. In the case of the high-k gate dielectric samples, a stacked structure (thin ALD-high-k film on thermally-grown SiO_2 film) was used to minimize the gate leakage current. We show that the crystallographic and surface morphological properties of the ALD-ZnO films strongly depend on the underlying gate dielectric layers, and also strongly correlate with the resulting TFT characteristics.

2 Experimental We fabricated typical bottom-gated TFTs with three different gate dielectric structures, including SiO_2 (300 nm), HfO_2 (50 nm)/SiO_2 (250 nm), and Al_2O_3 (50 nm)/SiO_2 (250 nm), on highly doped n-type Si (100) wafers. Initially, a 300-nm-thick SiO_2 layer was grown by a thermal oxidation process. For samples with high-k layers, the SiO_2 was etched down to a thickness of 250 nm using a buffered HF solution. This was done to maintain identical total physical thickness of the stacked gate dielectrics structures, which prevents increases in the gate leakage current. For the deposition of the Al_2O_3 and HfO_2 films,

thermal ALD was used at 300 °C using trimethylaluminium and tetrakis-(ethylmethylamino)hafnium metal-organic (MO) precursors, respectively, with H_2O oxidant. On all the samples, the ALD growth of 30-nm-thick ZnO channel layers was subsequently performed at 150 °C using diethylzinc (DEZn) and H_2O precursors. The fabrication of the ALD-ZnO TFTs was completed by patterning e-beam evaporated Au (80 nm)/Ti (10 nm) electrodes by an optical photolithography process. The ZnO-channel region was finally defined by UV photolithography and subsequent etching with a diluted HF solution. Before all of the following characterizations, post-deposition annealing (PDA) was performed at 300 °C for 3 min in oxygen ambient to control the carrier concentration in the ALD-ZnO films.

The crystal structures of the ALD-ZnO films were examined both by transmission electron microscopy (TEM) and by an X-ray diffractometer (XRD). Their surface morphologies and carrier densities were characterized by atomic force microscopy (AFM) and a Hall-effect measurement system, respectively. In addition, the surface polarity of the dielectric layers was measured by a contact angle measurement system. The electrical characteristics of the fabricated TFT devices were evaluated on the devices with a channel length of 10 μm and a width of 100 μm using a Hewlett-Packard 4145B semiconductor parameter analyzer.

3 Results and discussion First, in order to investigate the effect of the underlying dielectrics on the crystallographic evolution of the subsequently grown ALD-ZnO films, we obtained out-of-plane XRD patterns, which are shown in Fig. 1. For the ZnO films deposited on the amorphous dielectric layers (SiO_2 and Al_2O_3), only a strong (0002) reflection from the ZnO film was identified, revealing a preferentially oriented polycrystalline ZnO growth. Between these two samples, more preferential growth of the ZnO film occurred on the Al_2O_3 surface than on the SiO_2 surface. From the (0002) reflections of the ALD-ZnO films grown on SiO_2 and Al_2O_3 layers, full-width at half-maximum values of ∼0.48° and ∼0.3° were obtained, respectively, which implies a larger grain size of the ZnO film on Al_2O_3 than on SiO_2 according to the Scherrer's formula [12]. Unlike the ALD-ZnO film on the amorphous dielectrics, the ZnO film deposited on the polycrystalline HfO_2 (monoclinic phase) surface exhibited a randomly oriented polycrystalline nature, which was further verified by the following TEM analysis. This elucidates that the underlying polycrystalline HfO_2 film with a random orientation greatly affects the crystallinity of the subsequently deposited ZnO film.

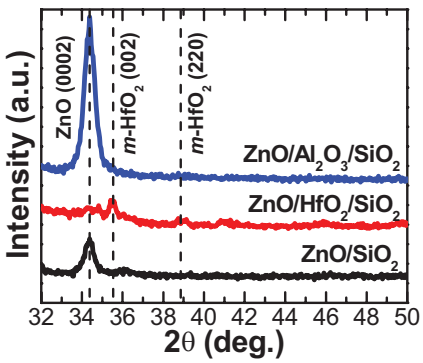

Figure 1 (online color at: www.pss-a.com) Out-of-plane XRD patterns obtained from the ALD-ZnO films grown on various gate dielectric layers. In the figure, *m* stands for a monoclinic phase.

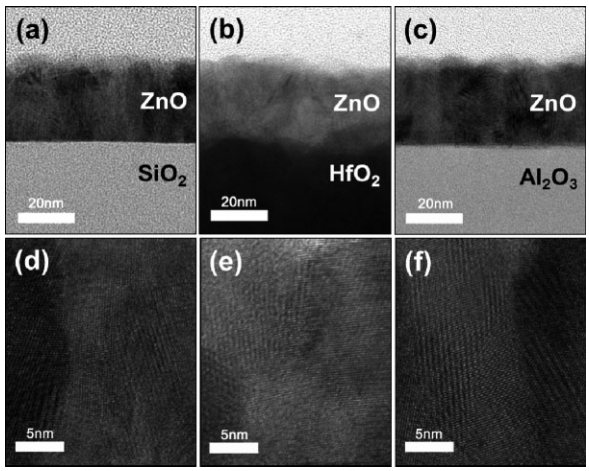

Figure 2 Cross-sectional TEM images of the ALD-ZnO films grown on various gate dielectric layers: (a and d) thermally grown SiO_2, (b and e) ALD-HfO_2, and (c and f) ALD-Al_2O_3 films. (d–f) are the enlarged ZnO film images of (a–c).

Once we found that the crystallographic properties of the ALD-ZnO layers are significantly influenced by the microstructures of the underlying dielectrics, detailed structural properties, and surface morphologies of the ZnO films were further investigated by taking cross-sectional TEM and surface AFM images, respectively (Figs. 2 and 3). Coinciding with the XRD result, a preferentially oriented columnar structure was observed in the ZnO film on the amorphous SiO_2 and Al_2O_3 layers, whereas a more randomly oriented polycrystalline structure was found on the partially crystallized HfO_2 layer, as shown in Fig. 2. More interestingly, the ZnO films deposited on the SiO_2 and Al_2O_3 dielectrics have much smoother surfaces than on HfO_2, which was also confirmed by an AFM measurement, shown in Fig. 3. The root-mean-square (rms) surface roughnesses of the ZnO film on SiO_2, Al_2O_3, and HfO_2 were ∼0.9, ∼0.6, and ∼3.4 nm, respectively. In contrast to the amorphous SiO_2

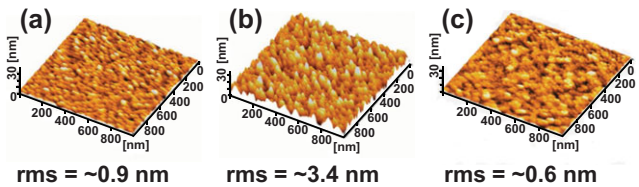

Figure 3 (online color at: www.pss-a.com) Surface morphologies of the ALD-ZnO films grown on various gate dielectric layers: (a) thermally-grown SiO_2, (b) ALD-HfO_2, and (c) ALD-Al_2O_3 films.

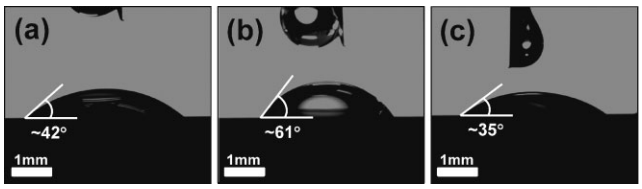

Figure 4 Contact angle measurement results on (a) thermally grown SiO_2, (b) ALD-HfO_2, and (c) ALD-Al_2O_3 films.

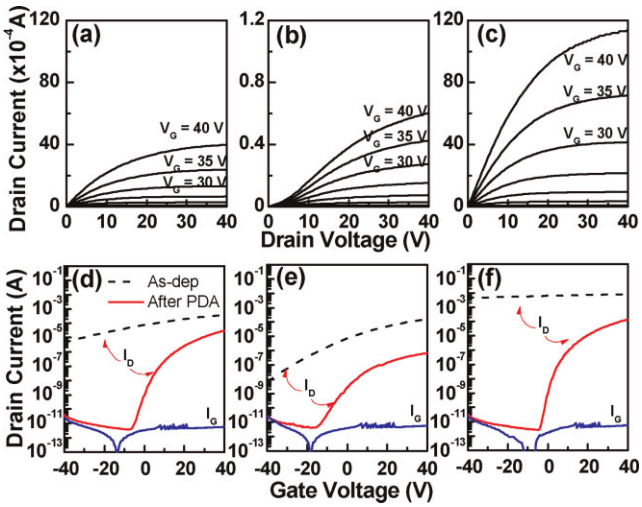

Figure 5 (online color at: www.pss-a.com) (a–c) Output and (d–f) transfer characteristics of the ALD-ZnO TFTs with (a and d) thermally grown SiO_2, (b and e) ALD-HfO_2, and (c and f) ALD-Al_2O_3 gate dielectrics. For the transfer characteristics, the drain voltage (V_D) was fixed at 10 V and the gate current (I_G) was measured from the sample after PDA.

and Al_2O_3 layers, which have smooth surface morphologies, the as-grown HfO_2 film has a rough surface due to its polycrystalline microstructure, which is believed to be directly transferred to the overlying ZnO layer due to the conformally depositing nature of the ALD-ZnO process.

In addition to the morphology of the starting surface, polarity is another important parameter that determines the consequential microstructural properties of the depositing film in a typical surface-adsorption activated ALD process [11]. Figure 4 presents the contact angle measurement results showing the images of water droplets on various dielectric surfaces. The contact angles were ~35° (on Al_2O_3), ~42° (on SiO_2), and ~61° (on HfO_2) in an ascending order, which can be explained by two possible origins: surface roughness and surface energy effects. The contact angle can increase as the surface gets rougher [13] and it matches well with the AFM result. In addition, the surface energies of amorphous Al_2O_3 (~700 mJ/m^2) [14] and SiO_2 (~300 mJ/m^2) [15] are higher than that of HfO_2 (~44 mJ/m^2) [16], which implies that surfaces of the Al_2O_3 and SiO_2 layers are much more hydrophilic than that of the HfO_2 layer. Since the hydrophilic surface has many hydroxyl (OH^-) groups that can easily react with ALD MO precursors [17], it is expected that the smooth Al_2O_3 surface can provide many preferential adsorption sites for the DEZn precursor during the ALD-ZnO process, which may incur well-oriented and large grain-sized ZnO film growth, as was observed in the XRD and TEM results. This explanation can also be applied to the observed differences in the ZnO crystallinity on SiO_2 and Al_2O_3 samples.

Figure 5 shows the output [drain current vs. drain voltage ($I_D - V_D$)] and transfer [I_D vs. gate voltage ($I_D - V_G$)] characteristics of the ALD-ZnO transistors fabricated on various dielectric structures. In addition, some of the device parameters extracted from the measured curves are listed in Table 1. Among the three fabricated samples, the ALD-ZnO transistor with an Al_2O_3 gate dielectric showed the best performance, as anticipated from the above-mentioned crystallographic properties and surface morphology. In typical polycrystalline semiconducting channel materials, the carrier mobility increases as the grain size increases because the large grains can minimize carrier scattering via defective grain boundaries [18]. Furthermore, the mobility in ZnO has an anisotropic property: the mobility along the *a*-axis is about twice as high as that along the *c*-axis [19]. Therefore, it can be expected that the highly *c*-axis-oriented ZnO film on Al_2O_3 with the largest grain size and smallest rms would exhibit the highest field-effect mobility compared to other samples, which agrees well with the measured data. In contrast, the lowest field-effect mobility is expected from the TFT with HfO_2, because the overlying ALD-ZnO film has a randomly oriented polycrystalline structure with small grains, as well as the worst interface morphology, which can act as an additional scattering center.

It needs to be mentioned that the carrier concentration estimated from the Hall-effect measurement in Table 1 shows an interesting trend with respect to the field-effect mobility. The increasing order of the field-effect mobility also follows that of the carrier concentration after PDA. For the single crystal semiconductors, a carrier concentration that is too high can reduce the carrier mobility as it provides

Table 1 Summary of the ALD-ZnO TFT parameters with various gate dielectric layers. The carrier density was measured by a Hall-effect measurement system.

gate dielectric	field effect mobility (cm^2/Vs)	subthreshold swing (V/decade)	$I_{on/off}$ ratio	carrier density after PDA (/cm^3)
SiO_2	~0.9	~2.26	~8×10^6	~2×10^{17}
HfO_2/SiO_2	~0.4	~4.45	~2×10^5	~9×10^{16}
Al_2O_3/SiO_2	~3.9	~1.35	~5×10^7	~8×10^{17}

more possibility for carrier-to-carrier scattering [20]. However, for the polycrystalline semiconductors, the relationship between the carrier concentration and mobility is quite complex due to the existence of critical carrier concentration (N^*) [21]. When the carrier concentration is above N^*, the barrier height at grain boundaries decreases, and mobility increases as a consequence. For instance, N^* of a poly-silicon film with a grain size of ~20 nm and a trap density of $3 \times 10^{12}/cm^2$ was computed to be $\sim 10^{18}/cm^3$, and its Hall mobility was relatively proportional to the carrier concentration in the range of 10^{18}–$10^{20}/cm^3$ [22]. Therefore, although precise information on N^* of ALD-ZnO is unavailable at this point, it is not unreasonable to expect higher mobility in the ZnO film with the highest carrier concentration on Al_2O_3 than that on other dielectric layers.

The carrier concentration is also closely related to the subthreshold swing (S), which is given by

$$S = \log(10)\frac{kT}{q}\left(1 + \frac{C_d + C_{it}}{C_{ox}}\right), \quad (1)$$

where k, T, q, C_d, C_{it}, and C_{ox} are the Boltzmann constant, temperature, unit charge, capacitance of depletion region, capacitance of interface traps, and capacitance of the gate dielectric, respectively. Hence, S in the ALD-ZnO TFTs is thought to be a combined result of carrier concentration (affecting C_d), interface trap density (affecting C_{it}), and the dielectric constant of the underlying gate dielectric (affecting C_{ox}). In this experiment, C_{ox} is the apparent value including the underlying SiO_2 film for the high-k/SiO_2 stacked structure, which can be approximated by assuming a serially connected capacitor structure. The ZnO TFT with Al_2O_3 has the highest carrier concentration as estimated from the Hall-effect measurement in Table 1 (hence, the highest C_d). However, it shows the lowest S because it has higher C_{ox} than SiO_2 and will probably have an overwhelmingly low interface trap density than HfO_2. Likewise, in spite of the highest C_{ox} value of HfO_2 and the lowest carrier concentration (hence, the lowest C_d), the ZnO TFT with HfO_2 resulted in the highest S because the rough interface will probably generate a significantly higher interface trap density than that of the ZnO TFT with Al_2O_3 or SiO_2. Note that high interfacial trapping states in the grain boundary can build up larger energy barrier height in the depletion region, affecting C_d and C_{it}. However, more work is needed on the effect of interface trap density in the future as it is beyond the scope of our present study.

4 Conclusion In summary, we fabricated and characterized bottom-gated ALD-ZnO TFTs with various gate dielectric structures including SiO_2, ALD-Al_2O_3, and ALD-HfO_2. When ALD-ZnO films were deposited, ALD-Al_2O_3 substrate resulted in the highest c-axis aligned crystallinity with the largest grain size and the best surface morphology, which were attributed to the lowest surface roughness with the most hydrophilic surface of the amorphous Al_2O_3. The microstructural and interface properties of the ALD-ZnO films affected by the underlying gate dielectrics largely determined the final TFT characteristics: the ALD-ZnO TFT with the ALD-Al_2O_3 showed the best transistor performance among others, including the highest field-effect mobility (~3.9 cm^2/Vs), the lowest subthreshold swing (~1.35 V/decade), and the highest on/off ratio ($\sim 5 \times 10^7$). These results emphasize the important technical implication in controlling the microstructure and interface of the ZnO layer by optimizing the underlying gate dielectrics for future high-performance display devices on flexible substrates.

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