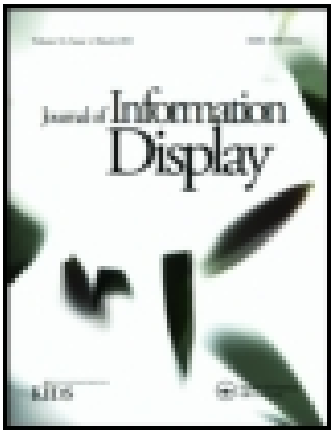

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Electrical performance of local bottom-gated MoS_2 thin-film transistors

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This paper reports the unique electronic properties of the local bottom-gated MoS_2 thin-film transistors (TFTs) fabricated on glass substrates. The current–voltage (*I–V*) characteristics of field effect transistors exhibited the on/off ratio of $\sim 1 \times 10^6$ and mobility higher than 20 $cm^2\ V^{-1}\ s^{-1}$. The doping concentration of MoS_2 flakes extracted by capacitance–voltage (*C–V*) measurement is approximately 10^{16}–10^{17} cm^{-3}. These results demonstrate that the electrical performance of the local bottom-gated TFTs are comparable with the conventional TFTs, providing important technical implications on the feasibility of MoS_2 TFTs.

Keywords: transition metal dichalcogenide; local bottom-gated; MoS_2; thin-film transistor

Introduction

Thin-film transistors (TFTs) in display backplanes have played an essential role in the development of display technologies. As displays require a larger screen size, a smaller form factor, and a higher resolution, the existing channel materials for TFTs, including amorphous silicon, organic semiconductors, low-temperature polysilicon (LTPS), oxide semiconductors, and graphene, have shown limitations such as low carrier mobility, incompatibility with large-area processes, high subthreshold swing, and low on/off ratio [1,2]. To overcome these difficulties, there is a rapidly growing interest in layered semiconductors composed of a transition metal and a chalcogen element [3,4]. Among these transition metal dichalcogenides (TMDCs), molybdenum disulfide (MoS_2) has been the most investigated because of its intriguing electrical and optical properties [5,6]. The recent reports on the MoS_2 TFTs indicated interesting electrical properties, including high field effect mobility, steep subthreshold slope for low power consumption, high on/off ratio, and electrical reliability [7–10]. These results suggest that MoS_2 can be a strong candidate for TFTs in the next-generation high-resolution liquid crystal displays (LCDs) and organic light-emitting diode (OLED) displays. There have been almost no reports, however, on the local bottom-gated MoS_2 TFTs, whose structures are widely used for the actual backplanes in LCDs and OLED displays. Therefore, in this paper, multilayer MoS_2 TFTs with a local bottom-gated structure are demonstrated. The local bottom-gated MoS_2 TFTs presented in this paper were fabricated using processes compatible with those of the conventional TFTs, and the electrical properties of such local bottom-gated MoS_2 TFTs were comparable with those of the conventional TFTs.

Device fabrication and experiments

Figure 1 shows a typical example of two-dimensional (2D) atomic layer-based materials for local bottom gated thin-film transistors. The local bottom-gated MoS_2 TFTs were fabricated as shown in Figure 2(a). First, gate electrodes (Ti ~10 nm/Au ~100 nm) were patterned on a glass substrate. This procedure formed the local bottom-gated structure. Then an amorphous ~100-nm-thick Al_2O_3 dielectric layer was deposited on the substrate via atomic layer deposition (ALD) using trimethylaluminum (TMA, UP Chemical Co. Ltd, South Korea) and H_2O as a precursor and a reactant. The deposition temperature was maintained at 300°C, and the gas injection schedule for one cycle of deposition was 0.5/10/1.5/15 s for the $TMA/N_2/H_2O/N_2$ gases [8]. The multilayer MoS_2 was transferred on the glass substrate from the bulk MoS_2 through mechanical exfoliation. Source/drain electrodes were patterned with Ti (10 nm)/Au (300 nm) using a lift-off method followed by photolithography. After the device fabrication, the TFTs were thermally annealed in a H_2 environment at 200°C for 2 h to improve the interface contact conditions between the metal and the semiconductor. The device structure of the fabricated local bottom-gated MoS_2 TFT was similar to those of the real

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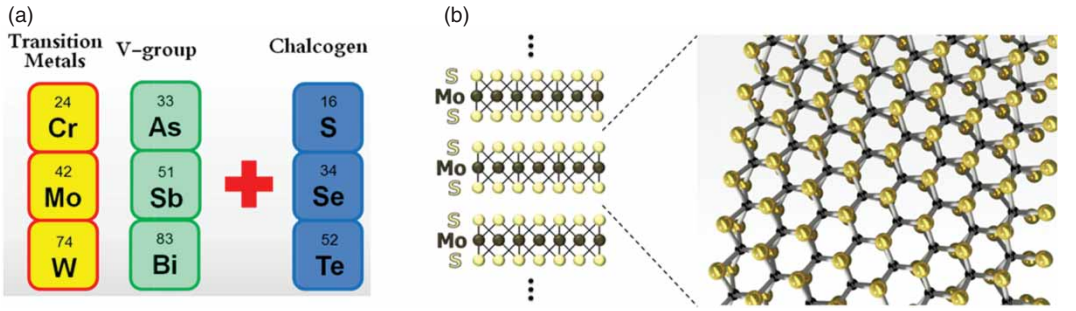

Figure 1. (a) Examples of constituting TMDCs. They are made through the formation of MX_2, where M = transition metal and X = chalcogen, and form a two-dimensional layered structure. (b) Schematic crystal structure of MoS_2.

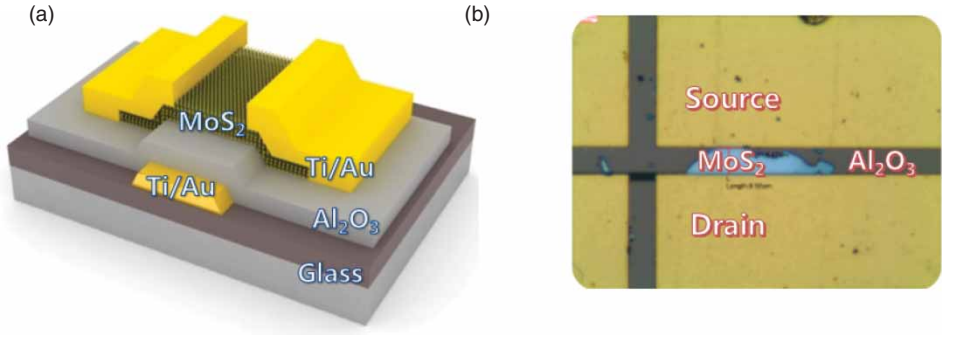

Figure 2. (a) Cross-sectional view of the multilayer MoS_2 TFT including an ALD Al_2O_3 gate insulator (100 nm) and patterned Ti/Au (10 nm/300 nm) S/D electrodes with a local bottom-gated structure. (b) Optical microscope image of the local bottom-gated MoS_2 TFT deposited on top of a glass substrate with a 100-nm-thick Al_2O_3 layer. The channel width and length of the TFT are 8.5 and 9.5 μm, respectively.

commercial device structures of the backplane TFTs in the OLED or LCD technology. An optical microscope image (Olympus BX51M) of the fabricated local bottom-gated MoS_2 TFT is shown in Figure 2(b). The as-exfoliated multilayer MoS_2 on the 100-nm-thick Al_2O_3 is between the source and drain electrodes with a 9.5 μm channel length. The patterned Ti/Au electrodes in the image were defined using photolithography, as mentioned earlier.

Results and discussion

I–V characteristics

The current–voltage (I–V) characteristics were measured to investigate the electrical device performances of the fabricated MoS_2 device. The I–V measurement was performed using the semiconductor characterization system (Keithley 4200 SCS) with a probe station in a local back-gated method, at room temperature. Figure 3 shows the electrical characteristics of the local bottom-gated MoS_2 TFT (gate length, ~9.5 μm; width, ~8.5 μm) with a 100-nm-thick ALD Al_2O_3 gate insulator. The transfer characteristics and the extracted mobility curve of the MoS_2 TFT are shown in Figure 3(a). The MoS_2 TFT exhibited a maximum transconductance ($g_m = dI_d/dV_{gs}|_{V_{ds}=1\,V}$) of 1.18 μS and showed an n-type behavior with an on- and off-current ratio (I_{on}/I_{off}) of $\sim 1 \times 10^6$. The field effect mobility of the MoS_2 transistor can be calculated as $\mu_{eff} = Lg_m/(WC_{ox}V_{ds})$, where L is the channel length, W is the channel width, and C_{ox} is the back-gate capacitance. The mobility extracted from the transfer curve was 21.4 $cm^2\,V^{-1}\,s^{-1}$ at the linear region (V_{ds} = 1 V).

Figure 3(b) shows the output curves (V_{ds}–I_d) of a representative MoS_2 transistor displaying n-channel transistor characteristics. It exhibited robust current saturation characteristics, as evidenced by the fact that the slope of each I_d curve was flat for a large V_{ds}. In Figure 3(c), the linear V_{ds}–I_d curve of the MoS_2 transistor indicates an Ohmic contact being established at the interface. These results show that the local bottom-gated MoS_2 TFT is comparable to the conventional TFTs, such as the amorphous Si, LTPS, or oxide TFT.

C–V characteristics

Figure 4 shows the capacitance–voltage (C–V) characteristics along the measurement setup. During the measurement, the source and drain contacts were grounded, as shown in Figure 4(a). Due to the very small area of the capacitor, noisy C–V curves were obtained at low frequencies (not shown). In the local bottom-gated structure, the existing parasitic capacitance, such as the pad capacitance, became negligible and, as such, only the pure channel capacitance was considered. The high-frequency C–V curves measured at 1 MHz

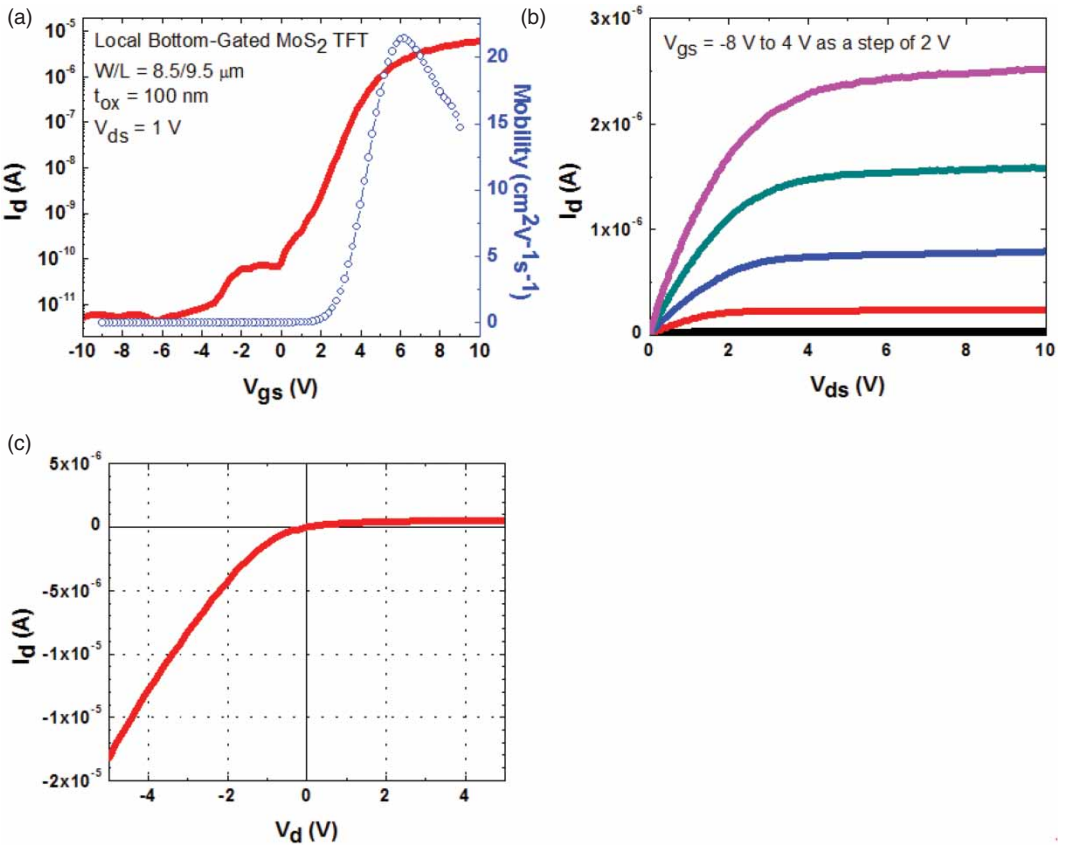

Figure 3. *I–V* characteristics of the local bottom-gated MoS_2 TFT. (a) Transfer curve measured under $V_{ds} = 1$ V and extracted mobility curve of the MoS_2 transistor. The field effect mobility at the linear region was 21.4 $cm^2/V\,s$, and the I_{on}/I_{off} was $\sim 10^6$. (b) Output characteristics of the MoS_2 transistor. The curves recorded for various back-gated voltages with a 2 V step. (c) Diode characteristics of the MoS_2 transistor.

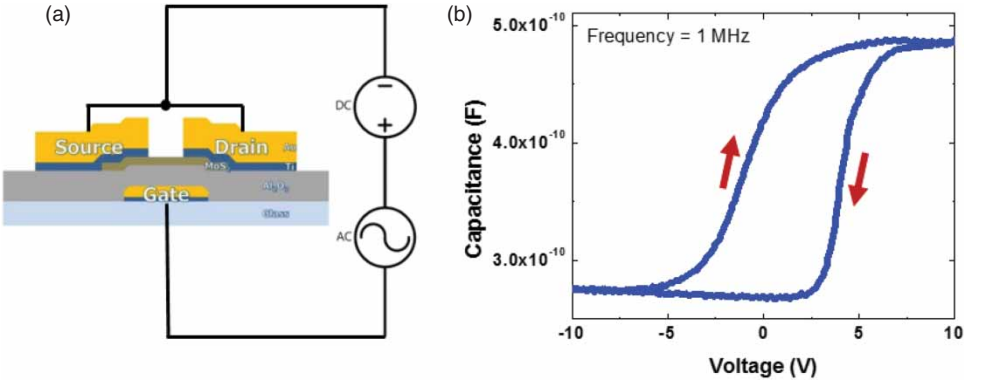

Figure 4. *C–V* measurement of the local bottom-gated MoS_2 TFT. (a) Schematic diagram of the *C–V* measurement setup. (b) Measured *C–V* curve of the MoS_2 transistor. The curve was measured under a frequency of 1 MHz.

are shown in Figure 4(b). They exhibit transition from accumulation to depletion as the gate voltage decreases, which is typically observed for an n-type metal-oxide-semiconductor capacitor. The hysteresis observed in the *C–V* curves (~5 V) is wider than that reported by Liu and Ye [11]. The nature of hysteresis can be speculated based on its direction: for the n-type capacitor, counterclockwise or clockwise hysteresis indicates that its dominant origin is mobile ions (or) charge injection. Also, the differences in the experimental conditions and device structure might have influenced the hysteresis as the primary origin of the hysteresis was the trapping states induced by the absorbed

water molecules on the MoS_2 surface [12,13]. The passivation of the MoS_2 channel layer will be able to significantly reduce the hysteresis. The doping concentration estimated from the *C–V* curves was $\sim 10^{16}$–$10^{17}\,cm^{-3}$, which well agrees with the figure reported in these authors' previous publication [8].

Conclusion

In summary, local bottom-gated TFTs were fabricated on glass via the mechanical exfoliation of MoS_2. The current–voltage (*I–V*) characteristics of the local bottom-gated TFTs showed a high on/off ratio of 1×10^6 and mobility exceeding $20\,cm^2V^{-1}\,s^{-1}$. The capacitance–voltage (*C–V*) characteristics measured at 1 MHz exhibited a typical n-type behavior with transition from accumulation to depletion. The doping concentration estimated from the *C–V* curves was $\sim 10^{16}$–$10^{17}\,cm^{-3}$. The results demonstrate that the electrical performance of the fabricated local bottom-gated MoS_2 TFTs is comparable with those of the real commercial TFTs used in the backplanes of LCD or OLED displays.

Funding

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