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High-temperature Electrical Behavior of a 2D Multilayered MoS_2 Transistor

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This paper reports the high-temperature-dependent electrical behavior of a 2D multilayer MoS_2 transistor. The existence of a big Schottky barrier at the MoS_2-Ti junction can reduce carrier transport and lead to a lower transistor conductance. At a high temperature (380 K), the field-effect mobility of the multilayer MoS_2 transistor increases to 16.9 $cm^2V^{-1}sec^{-1}$, which is 2 times higher than the value at room temperature. These results demonstrate that at high temperature, carrier transport in a MoS_2 with a high Schottky barrier is mainly affected by thermionic emission over the energy barrier.

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I. INTRODUCTION

For future display technologies, there are strong demands to provide high-resolution and mechanically-flexible flat panels, and significant progress has recently been achieved in improving high-performance flexible and foldable organic light-emitting diode (OLED) displays [1,2]. A conventional display consists of two major systems: a backplane to drive the OLED display device and address active-matrix pixels and a display device to create display images and movies. Sustained efforts to realize flexible backplanes have been reported for flexible and conformable thin-film transistors (TFTs), a core device to drive/switch active matrix display pixels [3–5]. However, conventional thin-film materials such as amorphous Si (α-Si), low-temperature poly Si (LTPS), and oxides, limit the use of such TFTs in flexible backplane-circuitry due to their fragility and relatively low mobility.

Two-dimensional (2D) layered semiconducting chalcogenides (such as MoS_2, $MoSe_2$, WS_2, WSe_2, *etc.*) have attracted much attention due to their having an intrinsically high carrier mobility (> 100 $cm^2V^{-1}s^{-1}$), mechanical flexibility for a 2D layered structure, and a finite bandgap ($\sim$1.35 eV) [6–8]. For a high-performance 2D layered semiconducting transistor, recent reports suggest that Ti was selected from among the low work function materials because its favorable interface geometry Ti allows bonding and the electronic density of states (DOS) at the Fermi level to be maximized through an increase in the overlap between the states at the interface [9]. However, such improvements for the transistors to date have fundamentally been hampered by the presence of a Schottky barrier at the 2D layered MoS_2-Ti metal junction. A natural bulk MoS_2 crystal (SPI supplies, USA) is typically found in the '2H phase', what has a semiconducting property, but often contains the '3R phase', what shows a semi-metallic behavior [10]. This is because of the doping concentration and the chirality in the natural MoS_2 crystal, which can not to be controlled exactly. Previous reports on MoS_2 transistors show outstanding electrical properties, including high performance and a low subthreshold slope [4], but some of those devices fabricated till to date have contained a high Schottky barrier at the MoS_2-Ti metal junction after H_2 annealing, and the presence of the Schottky barriers severely blocks carrier transport in the channel and limits the transistor performance matrix.

In this research, we investigated the high-temperature electrical behavior of a MoS_2 transistor with a high Schottky barrier. From experimental temperature-dependent current-voltage (IV) measurements, the extracted field-effect mobility of the MoS_2 transistor was found to be proportional to the temperature. The carrier mobility in a typical MoS_2 crystal is limited by optical phonon scattering at high temperature, but the present immature MoS_2 transistors, as opposed to ohmically-contactedMoS_2 transistors, show an enhanced mobility at high temperature. High temperature leads to a larger thermionic emission that transports electrons over the energy barrier. Furthermore, the carrier transport mechanism and the calculation of Schottky barrier in the multilayer MoS_2 devices are discussed based on the observations.

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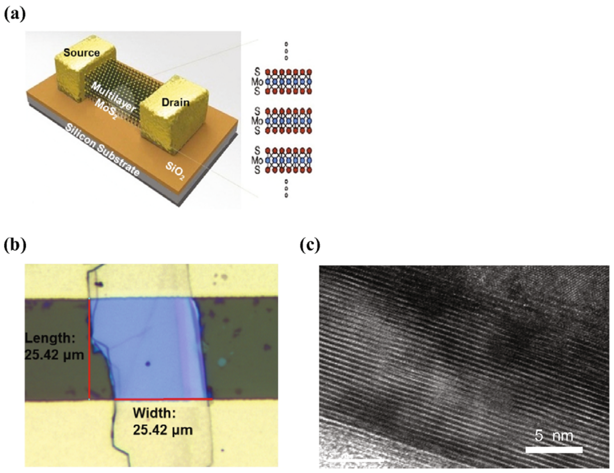

Fig. 1. (Color online) (a) Schematic diagram of a 2D multilayered MoS_2 TFT with a back-gated structure. (b) Optical microscope image of this device. (c) Bright-field TEM image of the layered structure. A monolayer generally has a thickness of 1nm.

II. MULTILAYER MOS_2 TRANSISTOR AND ELECTRICAL CHARACTERISTICS

Figure 1(a) shows a cross-sectional view of a 2D multilayered MoS_2 transistor with a back-gated structure, where a highly-p-doped Si wafer (resistivity $< 5 \times 10^{-3}$ Ω·cm) is utilized as a common back and is covered with a 300-nm-thick SiO_2 layer as a gate dielectric. The fabrication begins with mechanical exfoliation of the MoS_2 layers from bulk MoS_2 crystals (SPI supplies, USA), and then transfers them onto a thermally-grown SiO_2 layer. After the mechanical exfoliation of a multilayer MoS_2 crystal, the sample is annealed in a vacuum tube at 200 °C for 2 hours (100 sccm Ar and 10 sccm H_2) to remove the tape residue on the surface of the MoS_2 and to lower the contact resistance in the MoS_2-Ti/Au junction. Finally, Ti/Au (20 nm/300 nm) metals for S-D electrodes are deposited by using e-beam evaporation and are patterned by using photolithography, with a channel length of 11.47 μm. Figure 1(c) shows the bright-field transmission electron microscopy (TEM) image of the layer-by-layer structure, where each layer is weakly held together by Van der Waals interactions.

First, the electrical characteristics of an as-fabricated MoS_2 TFT were measured at room temperature. Figure 2(a) shows the drain current versus gate-source voltage (I_d-V_{gs}) of this device at a drain voltage Vds = 1 V. The MoS_2 transistor exhibits the on/off current ratio $(I_{on}/I_{off}) \sim = 10^6$ and a threshold voltage $V_{th} = -11$ V. The field-effect mobility (μm) deduced from the maximum transconductance ($g_m = dI_d$ / dV_{gs} at $V_{ds} = 1$ V) of 0.1 μS is 8.93 $cm^2V^{-1}s^{-1}$ at room temperature. Figure 2(b) shows typical output characteristics (I_d-V_{ds}) under various gate voltages in steps of 7 V for the multilayer MoS_2. The I_d-V_{ds} curves are close to those of a conventional n-channel metal oxide semiconductor (NMOS) transistor, having a linear triode region at low V_{ds} and a saturation region at high V_{ds}. The drain current at high V_{ds} is observed to fully saturate for all gate voltages.

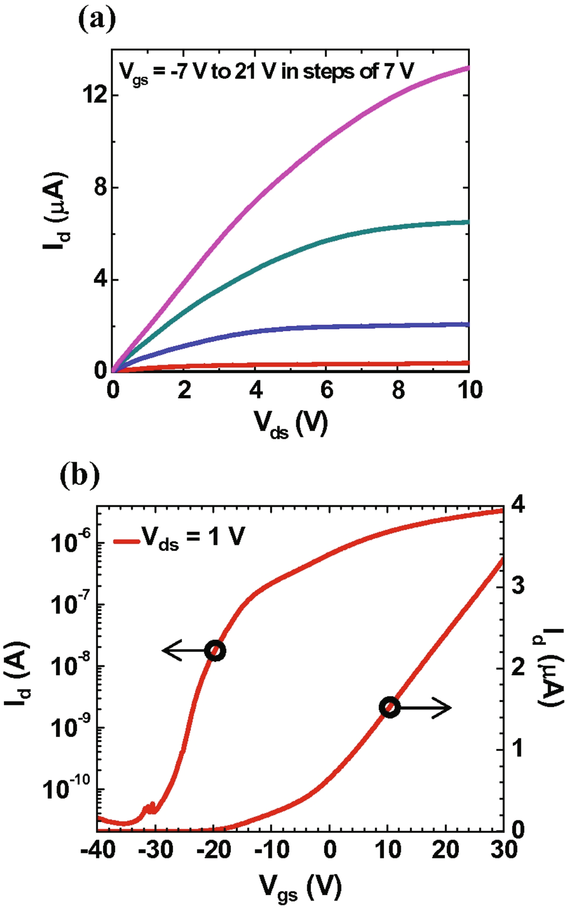

Fig. 2. (Color online) Measured electrical characteristics of a depletion-mode n-type MoS_2 transistor at room temperature: (a) drain current versus drain bias (output curve) with respect to gate bias, and (b) drain current versus gate-source voltage at V_{ds} = 1 V on a log scale and a linear scale.

III. TEMPERATURE DEPENDENT IV CHARACTERISTICS OF A MOS_2 TRANSISTOR

To investigate the temperature-dependent carrier transport mechanism, we measured the electrical characteristics of the device as a function of temperature (300 to 380 K), as shown in Fig. 3. The carrier mobility is intrinsically determined by the scattering mechanism, such as scattering from the Schottky barrier and from, ionized impurities and optical phonon scattering. Our reported result demonstrates that for a well-designed MoS_2 transistor, having a relatively low Schottky barrier, the scattering mechanism is dominated by enhanced

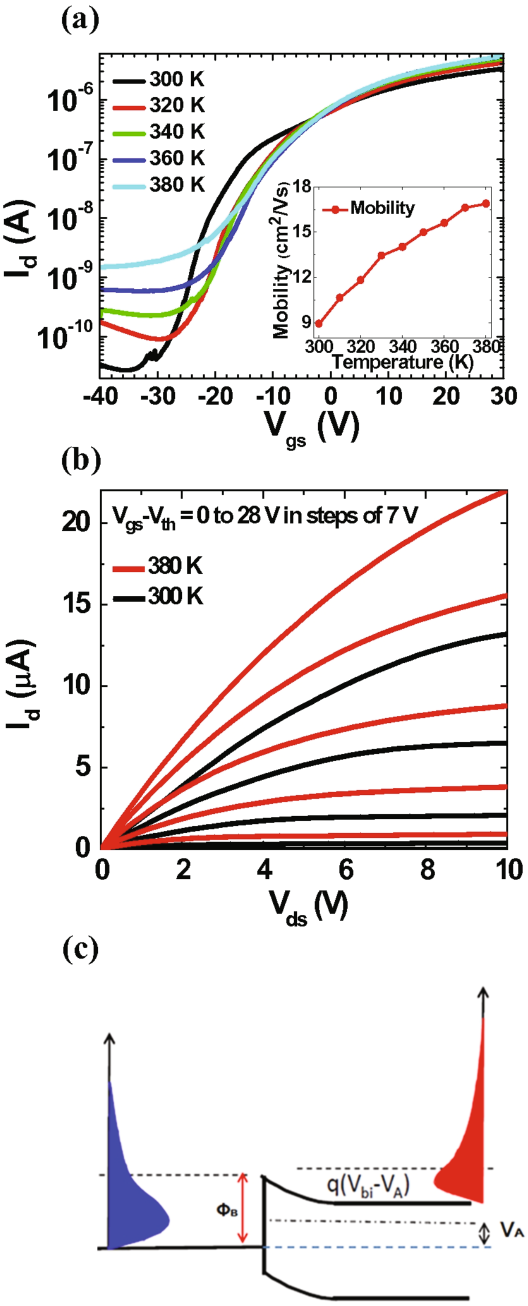

Fig. 3. (Color online) Electrical characteristics of a 2D multilayer MoS_2 transistor for various temperatures. (a) The I_d-V_{gs} characteristics of a representative device. The inset shows the temperature-dependent field-effect mobility at temperatures from 300 K to 380 K in steps of 10 K. (b) I_d-V_{gs} characteristics for V_{gs}-V_{th} at room temperature (black line) and high temperature of 380 K (red line). (c) Energy band diagram and carrier distribution at the Schottky barrier between the MoS_2 semiconductor and the Ti/Au metal.

optical-phonon and acoustic- phonon scattering above room temperature. Thus, the extracted field-effect mobility of a good device should be inversely proportional to the temperature. However, the mobility behavior of the device (Fig. 3(a)) is fully contradictory with that of the previous good device; the mobility of the present MoS_2 transistor (μm < 10 $cm^2V^{-1}s^{-1}$) is proportional to the temperature. At high temperature, the lattice vibration limits the carrier mobility at the ohmically-contacted 2D MoS_2 transistor, but the transport of electrons on this device is strongly limited by the thermionic emission over the potential barrier due to the large Schottky barrier (Φ_B) at MoS_2-Ti/Au junction. The current due to thermionic emission in a representative MoS_2 transistor, as shown in Fig. 3(c), is given by

$$J_T = A * T^2 * e^{\frac{-q\Phi_B}{kT}}[e^{\frac{qV_A}{kT}} - 1], \tag{1}$$

where Φ_B is the Schottky barrier height, V_A is an applied bias, and the parameter A is the effective Richardson constant. The above equation shows that the probability of carriers going over the potential barrier is enormously increased as the temperature is increased, thus, a larger total current (J_T) leads to a higher mobility at higher temperatures. The carrier transport in the present transistor with a high Schottky barrier is strongly limited by thermionic emission; thus, the mobility at high temperature (380 K) is increased to 16.9 $cm^2V^{-1}s^{-1}$, which is 2 times higher than that at room temperature.

IV. CONCLUSION

In conclusion, the high-temperature-dependent carrier transport of a MoS_2 transistor with a high contact resistance is investigated. By comparing the transistor is mobility with increasing operation temperature, we found the μm to be limited by thermionic emission at high operation temperature due to the high Schottky barrier at the MoS_2-Ti/Au metal junction. In this regards, a high-performance 2D multilayer MoS_2 transistor having a zero or slightly negative Schottky barrier can be realized. Furthermore, the observing the high-temperature electrical behavior will be a good method for determining whether the device is an ohmically-contacted or a large-Schottky-barrier device.

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