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Nanowire-based ternary transistor by threshold-voltage manipulation

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We report on a ternary device consisting of two nanowire channels that have different threshold voltage (V_{th}) values and show that three current stages can be produced. A microscale laser-beam shot was utilized to selectively anneal the nanowire channel area to be processed, and the amount of V_{th} shift could be controlled by adjusting the laser wavelength. Microscale laser annealing process could control V_{th} of the individual nanowire transistors while maintaining the other parameters the constant, such as the subthreshold slope, on–off current ratio, and mobility. This result could provide a potential for highly integrated and high-speed ternary circuits. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4871413]

Integrating high-density electronic circuits, increasing computational efficiency, and reducing the device size are critical requirements for developing existing and future electronics. In this sense, multivalued logic circuits, especially ternary devices, are proposed to solve the above issues. In contrast to binary logic circuits currently used in all electronic circuitry, ternary logic circuits could contribute to the increase in the degree of integration of the devices by decreasing the number of devices that make up the logic blocks.[1–4] The decrease in the number of devices may reduce the parasitic effect and consequently increase tolerance to noise. Moreover, data processing can be accelerated because ternary logic circuits could process a large volume of data in a short time. Considering these advantages, ternary logic circuits should be considered as one of the most important research topics in the investigation of next-generation complementary metal–oxide semiconductor circuits.

To fabricate ternary devices, the operating voltages must be categorized into three levels. One of the fabrication methods of ternary devices involves the use of two semiconductor channels. Because the threshold voltage (V_{th}) values of the two semiconductor channels must be different from each other, V_{th} must be capable of being selectively shifted to only one semiconductor channel. In addition, a method should be developed to accurately produce a positive shift in V_{th} according to the original design plan. Furthermore, only V_{th} should be shifted while the other transistor characteristics must be maintained constant, such as the on-current (I_{on}), subthreshold slope (SS), on–off current ratio (I_{on}/I_{off}), and field-effect mobility (μ_{eff}). Many studies have been conducted so far to control V_{th}. In some previous studies, thermal annealing, ultraviolet (UV), UV-ozone (UVO), and plasma treatments were implemented to control V_{th}.[5–8] Moreover, excimer and femtosecond lasers were used to achieve V_{th} control.[9,10] However, two major limitations were encountered in these approaches: (i) the other transistor characteristics such as I_{on}, SS, I_{on}/I_{off}, and μ_{eff} changed along with the change in V_{th} after the processes, and (ii) a selective transistor characteristic change in only the semiconducting channel could not be achieved, because some of the methods should be employed to the entire substrate. Thus, these methods are not sufficient to fabricate ternary devices.

In this study, a selective laser anneal on a nanowire channel was implemented to control the V_{th} shift. The amount of change in V_{th} of a SnO_2 nanowire transistor was investigated by varying the laser wavelength. The semiconducting nanowires could have different V_{th} values by using a micro-scale laser annealing process. Using our proposed method, we fabricated a ternary device which showed three current stages.

A ternary device consisting of two bottom-gate structural transistors was fabricated using a SnO_2 nanowire as a semiconductor channel and an atomic layer-deposited Al_2O_3 ($T_{ox} = 30$ and 70 nm) as a gate insulator. The SnO_2 nanowires with band gap (E_g) of ~3.6 eV at 300 K were synthesized by chemical vapor deposition.[11] The average diameter and length of the SnO_2 nanowires were 30 nm and over 10 μm, respectively. The gate and source–drain electrodes were formed using a sputtered ITO thin film (100 nm) by a lift-off process.

A pulsed Nd:YAG laser (Surelite III-10, Continuum, Inc.) was operated at two different wavelengths (266 and 532 nm). The laser annealing process was performed in ambient air. The laser was exposed only to the nanowire channel region using a microlevel laser shot system. The nanowire channel area could be observed through a microscope in the laser shot system during the laser annealing process, and the target exposed position and beam spot size (2–8 μm) could be adjusted using a micro-xyz stage.

The transistor characteristics were measured using a semiconductor parameter analyzer (Agilent B1500A). μ_{eff} was derived from the calculated gate-to-channel capacitance $C_i = 2\pi\varepsilon_0 k_{eff} L/\cosh^{-1}(1 + t_{ox}/r)$ using $\mu_{eff} = dI_{ds}/dV_{gs} \times L^2/C_i \times 1/V_{ds}$. The effective dielectric constant of Al_2O_3 (k_{eff}), the channel length (L), and the radius (r) of the SnO_2 nanowire were 9.0, 2.4 μm, and 15 nm, respectively. The statistical data of the devices were calculated from the

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measured transistor characteristics in terms of V_{th} (V_{gs} at $I_{ds} = 10\,nA$ and $V_{ds} = 1.0\,V$), I_{on} (I_{ds} at $V_{gs} = V_{th} + 2\,V$ and $V_{ds} = 1.0\,V$), and off-current (I_{off} at $V_{ds} = 1.0\,V$ and average I_{ds} of the five-point I_{ds} from the off-region).

Figure 1 shows the schematic diagram of the laser annealing on the SnO_2 nanowire channel area in the bottom-gate nanowire transistor. The insets in Fig. 1 show the microscope image, which was obtained during a laser shot, and the field emission scanning electron microscope (FE-SEM) image of the nanowire channel region. The length and diameter of the single SnO_2 nanowire between the source–drain electrodes were $\sim$2.4 μm and $\sim$30 nm, respectively. Two different laser wavelengths (266 and 532 nm) with laser fluence values of 0.34 and 0.12 J/cm^2, respectively, and a 2-s exposure time were employed. The beam spot diameter was $\sim$2.0 μm. The unique aspect of the selective laser annealing process is that the laser can be directed only on the nanowire channel region without affecting the other areas, especially the nanowire source–drain contact areas. Typical thermal treatment or plasma treatment may produce undesirable effects because it is applied to the entire substrate. In addition, because thermal treatment is performed at 400–900 °C for 30–120 min, the method cannot be used for devices that must be fabricated on plastic substrates. However, the selective laser annealing process employed in our study provides a solution to the above problems on the basis of its advantages: the annealing treatment can be carried out for only the targeted areas in a selective manner, and laser illumination for a short period of time reduces the process time and minimizes any possible thermal damage to the substrate.

The log-scale drain current versus gate–source voltage (I_{ds}–V_{gs}) characteristics of the single SnO_2 nanowire transistor at $V_{ds} = 1.0\,V$ before (black square) and after (red circle) laser annealing at two wavelengths (266 and 532 nm) are shown in Fig. 2. Figure 2(a) shows the representative I_{ds}–V_{gs} characteristics of the SnO_2 nanowire transistor under a 532-nm laser annealing process with a laser fluence of 0.12 J/cm^2 and an exposure time of 2 s. Before laser annealing, the SnO_2 nanowire transistor exhibited $V_{th} = 1.34\,V$, SS = 0.5 V/dec, $I_{on}/I_{off} = 3.26 \times 10^6$, $I_{on} = 2.31 \times 10^{-6}$ A, and $\mu_{eff} = 14\,089$ cm^2/V·s. After laser annealing, the same device showed a positively shifted $V_{th} = 2.10\,V$ while maintaining similar values—SS = 0.5 V/dec, $I_{on}/I_{off} = 2.73 \times 10^6$, $I_{on} = 3.47 \times 10^{-6}$ A, and $\mu_{eff} = 15\,004$ cm^2/V·s. Figure 2(b) shows the representative I_{ds}–V_{gs} characteristics of the SnO_2 nanowire transistor under a 266-nm laser annealing process with a laser fluence of 0.34 J/cm^2 and an exposure time of 2 s. The as-fabricated SnO_2 nanowire transistor showed $V_{th} = 1.32\,V$, SS = 0.7 V/dec, $I_{on}/I_{off} = 1.31 \times 10^6$, $I_{on} = 6.25 \times 10^{-7}$ A, and $\mu_{eff} = 3378$ cm^2/V·s; whereas the SnO_2 nanowire transistor treated with laser annealing exhibited a positively shifted $V_{th} = 3.52\,V$ while maintaining similar values of SS = 0.8 V/dec, $I_{on}/I_{off} = 1.21 \times 10^6$, $I_{on} = 5.03 \times 10^{-7}$ A, and $\mu_{eff} = 3589$ cm^2/V·s. As a result, the V_{th} showed a positive shift of 0.76 V (532 nm) and 2.20 V (266 nm) without any major changes in the SS, I_{on}/I_{off}, and I_{on} values.

In the case of the oxide nanowire transistors, thermal annealing, UV, UVO, or plasma treatment produces a negative or positive V_{th} shift.[5–10] Moreover, some treatment processes could restore V_{th} to its original state. In this context, we verified in this study whether the V_{th} characteristic can

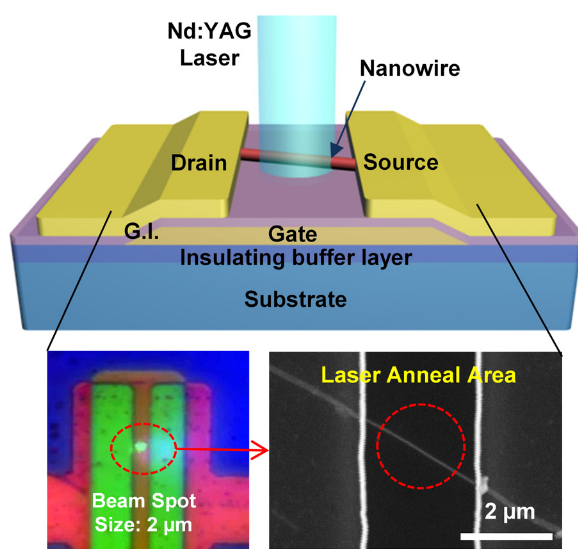

FIG. 1. Schematic diagram of a single SnO_2 nanowire transistor. The channel region of the nanowire was exposed to a pulsed Nd:YAG laser (laser fluence: $\sim$0.34 J/cm^2 (266 nm) and 0.12 J/cm^2 (532 nm)). The inset shows the top view of the microscopic image of the device area with a laser shot on only the nanowire channel region. The laser spot size was 2 μm. The other inset shows the FE-SEM image of the nanowire channel region. The scale bar is 2.0 μm.

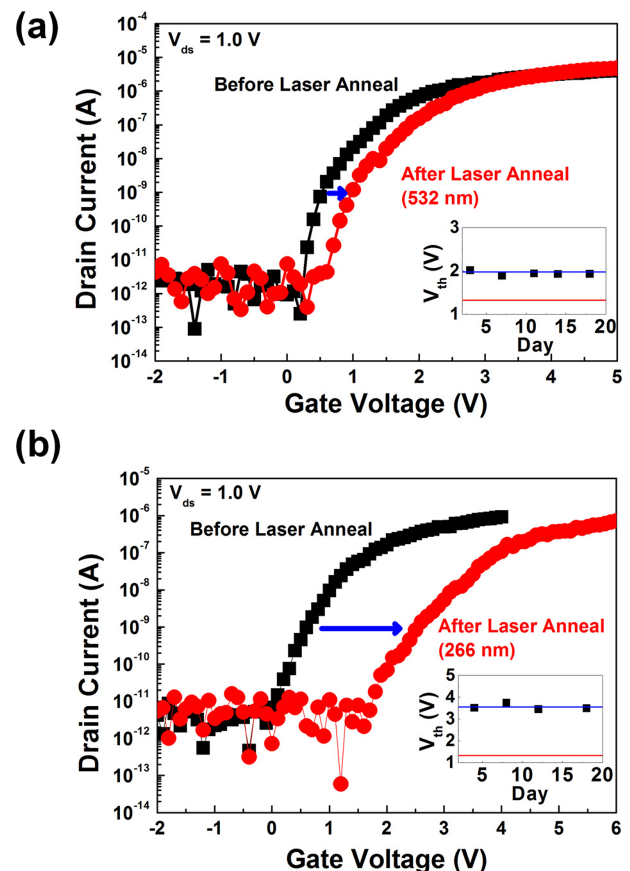

FIG. 2. (a) I_{ds}–V_{gs} characteristics of the SnO_2 nanowire transistor before and after the laser annealing process (532 nm). (b) I_{ds}–V_{gs} characteristics of the SnO_2 nanowire transistor before and after the laser annealing process (266 nm).

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be maintained or restored after the laser annealing process. The insets in Figs. 2(a) and 2(b) show the change in the transistor characteristics after a lapse of time after laser annealing. As shown in the figures, the transistor characteristics remained the same even after 18 days.

The most prominent effect of laser annealing is the control of the V_{th} shift by adjusting the laser wavelength. The V_{th} shift after the 532-nm laser annealing process exhibited a small change, but it displayed a large change after the 266-nm laser annealing process. On the other hand, the unchanged transistor characteristics—i.e., SS, I_{on}/I_{off}, and I_{on}—after laser annealing indicated that the laser annealing process did not cause degradation in the nanowire at the interface states. In other words, the surface states in the nanowires did not increase during laser annealing. There are several methods to improve the SS of an oxide nanowire transistor: (i) reducing the thickness of the gate insulator,[12] (ii) using the gate insulator which has a high dielectric constant,[12] and (iii) controlling the interface between gate insulator and semiconductor nanowire channel.[7,13] On the other hand, only the V_{th} shifted without degrading the other transistor characteristics following the decrease in the oxygen vacancies (V_o, V_o^+, and V_o^{++}).[14,15] The laser anneal, which was applied in this study, was exposed only on nanowire channel surface in ambient air. The oxygen ions generated from the laser annealing process in ambient air then filled the oxygen vacancies and reduced the final amount of V_o. Because V_o, V_o^+, and V_o^{++} play the role of electron-trapping sites, a decrease in such sites leads to a positive V_{th} shift in the N-type oxide nanowire transistors.[16] The laser anneal process could change the amount of oxygen vacancies on nanowires, but might not affect the interface state between gate insulator and nanowire. For this reason, V_{th} of the device was shifted without changing SS.

The changes in V_{th}, SS, I_{on}/I_{off}, and I_{on} in the SnO_2 nanowire transistors in six devices before and after laser annealing were measured, and the average and standard deviations are shown in Fig. 3. After laser annealing at 266 nm, V_{th} showed a positive shift of 2.02 ± 0.51 V. On the other hand, laser annealing at 532 nm produced only a positive shift of 0.33 ± 0.25 V, which was a relatively slight change. Thus, the decrease in the wavelength led to the increase in the amount of positive shift. We assume that this phenomenon occurred because the lower wavelength (266 nm and 4.66 eV) of the laser reacted more actively with the surface of the SnO_2 nanowire (bandgap of 3.6 eV) in ambient air than the higher wavelength (532 nm and 2.33 eV), consequently filling up the oxygen vacancies with oxygen. Meanwhile, the SS, I_{on}/I_{off}, and I_{on} values showed no significant changes after laser annealing at the two laser wavelengths (266 and 532 nm). The SnO_2 nanowire transistors after laser annealing exhibited unchanged average values of ΔSS (0.00 ± 0.21 V/dec (266 nm) and -0.10 ± 0.09 V/dec (532 nm)), $\Delta(I_{on}/I_{off})$ ($(-0.23 \pm 0.19) \times 10^6$ (266 nm) and $(-0.18 \pm 0.43) \times 10^6$ (532 nm)), and $\Delta I_{on} = ((-0.74 \pm 1.21) \times 10^{-6}$ A (266 nm) and $(0.17 \pm 0.49) \times 10^{-6}$ A (532 nm)). Note that deviation (Δ) is the difference between the unannealed value and the annealed value.

As an application of our capability to adjust the V_{th} values of individual SnO_2 nanowires, we fabricated a ternary

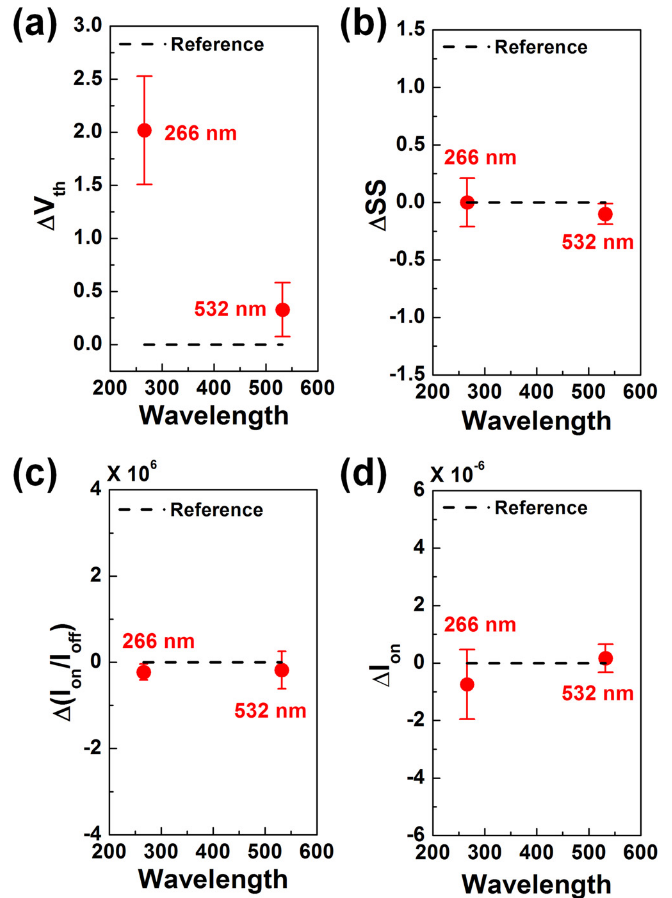

FIG. 3. Variations in the (a) threshold voltage, (b) subthreshold slope, (c) on–off current ratio, and (d) field-effect mobility of the SnO_2 nanowire transistors after the laser annealing process at different wavelengths (266 and 532 nm).

device. Two methods are available to encode and operate the ternary devices using ternary variables: (i) unbalanced ternary encoding with three values [0, 1, and 2] of the ternary variable, and (ii) balanced ternary encoding with three values [−1, 0, and 1] of the ternary variable. Nd:YAG laser annealing with a microscale beam spot size introduced here appears to be the ideal method for fabricating the ternary transistor to control V_{th}. Figure 4(a) shows the FE-SEM image of the representative ternary device consisting of two SnO_2 nanowire channels with different V_{th} and I_{on} values. Nd:YAG laser annealing (266 nm and 0.34 J/cm^2) for 2 s was carried out in only one nanowire channel (NW_2) out of the two nanowire channels (NW_1 and NW_2). As a result, the laser-annealed device showed a V_{th} of 3.0 V whereas the other nanowire transistor that did not undergo laser annealing showed a V_{th} of 0.1 V. The laser anneal method which was introduced in this study can only manipulate V_{th}. Thus, I_{on} level should be controlled by changing the thicknesses of gate insulators on unannealed and annealed nanowire channel regions. The 70-nm-thick and 30-nm-thick Al_2O_3 thin films were utilized on the unannealed and annealed transistors, respectively. The nanowire with the low I_{on} was selected on the unannealed channel region and the nanowire with the high I_{on} was treated with the laser anneal.

Figure 4(b) shows the log-scale I_{ds}–V_{gs} of the ternary device. The two transistor characteristics with different V_{th}

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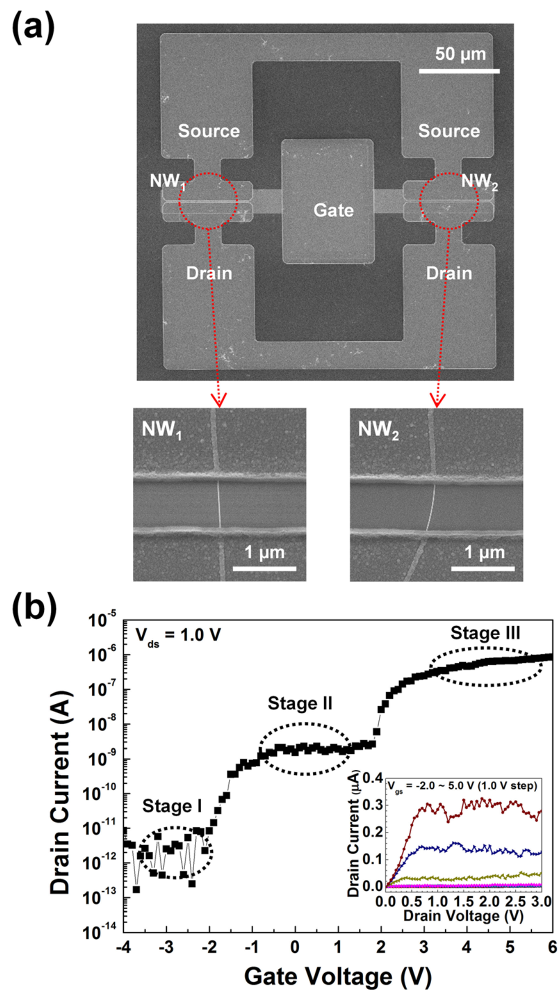

FIG. 4. Ternary device. (a) FE-SEM image of the ternary device based on two n-type SnO_2 nanowire transistors. The scale bar is 100 μm. The inset shows the representative nanowire channel regions of the transistors; the scale bar is 10 μm. (b) I_{ds}–V_{gs} characteristics of the ternary device. The inset shows I_{ds}–V_{ds} characteristics of the ternary device.

values combined to exhibit a device characteristic with three current levels. In other words, three different current stages of $\sim 3 \times 10^{-12}$ A (stage I), $\sim 1.5 \times 10^{-9}$ A (stage II), and $\sim 6 \times 10^{-6}$ A (stage III) exist at below -2 V, from -1.1 to 1.8 V, and over 2.8 V, respectively. The inset in Fig. 4(b) shows the drain current versus drain-to-source voltage (I_{ds}–V_{ds}) characteristics of a representative ternary device with a V_{gs} range from -2.0 to 5.0 V in 1.0 V steps and after laser annealing. One current group had a value of $\sim$4 nA at $V_{ds} = 1.0$ V and $V_{gs} = 1.0$ V, and the other group had a value of $\sim$0.29 μA at $V_{ds} = 1.0$ V and $V_{gs} = 5.0$ V.

In conclusion, we fabricated a ternary device by combining two SnO_2 nanowire channels with different V_{th} values. Controlling the V_{th} of the nanowires is of primary importance in the fabrication of nanowire-based ternary devices. To control the amount of V_{th} shift, a Nd:YAG laser annealing process at two wavelengths (266 and 532 nm) was implemented. Microscale laser annealing could focus and tune only the individual nanowire channels. We expect that the direct illumination of nanowires could prevent damage to the nanowires during the laser annealing process. On the basis of the result of laser annealing at two different wavelengths, the laser illumination at the 266-nm wavelength produced more positive shifts of V_{th} than that at the 532-nm wavelength. The positive V_{th} shift originated from the reduced number of oxygen vacancies on the surface of the oxide nanowire. As a result, we controlled V_{th} through the microscale laser annealing process while maintaining the SS, I_{on}/I_{off}, I_{on}, and μ_{eff} characteristics. Therefore, the suggested trimming method in this study is expected to provide a powerful and effective means of manufacturing a variety of nanowire-based integrated circuits.

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