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Electrical characteristics of multilayer MoS_2 transistors at real operating temperatures with different ambient conditions

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Atomically thin, two-dimensional (2D) materials with bandgaps have attracted increasing research interest due to their promising electronic properties. Here, we investigate carrier transport and the impact of the operating ambient conditions on back-gated multilayer MoS_2 field-effect transistors with a thickness of ~50 nm at their realistic working temperatures and under different ambient conditions (in air and in a vacuum of $\sim10^{-5}$ Torr). Increases in temperature cause increases in I_{min} (likely due to thermionic emission at defects), and result in decreased I_{on} at high V_G (likely due to increased phonon scattering). Thus, the I_{on}/I_{min} ratio decreases as the temperature increases. Moreover, the ambient effects with working temperatures on field effect mobilities were investigated. The adsorbed oxygen and water created more defect sites or impurities in the MoS_2 channel, which can lead another scattering of the carriers. In air, the adsorbed molecules and phonon scattering caused a reduction of the field effect mobility, significantly. These channel mobility drop-off rates in air and in a vacuum reached 0.12 cm^2/V s K and 0.07 cm^2/V s K, respectively; the rate of degradation is steeper in air than in a vacuum due to enhanced phonon mode by the adsorbed oxygen and water molecules. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4898584]

Two-dimensional (2D) materials are enabling the development of new electronics technologies for next-generation nanoelectronic devices. Among 2D materials, graphene has been studied the most and has attracted the most attention because of its outstanding mechanical, optical, and electrical properties, as well as its processability.[1–3] Despite these excellent properties, graphene's major drawback is its gapless band structure, which makes it difficult to use in electrical switching devices such as transistors. Furthermore, a great amount of effort to achieve a sufficient bandgap has created other issues, increasing fabrication complexity and reducing mobility.[4,5]

Especially, molybdenum disulfide (MoS_2), a layered transition-metal dichalcogenide material composed of vertically and weakly stacked layers held together by van der Waals interactions, has several advantages to use as the active channel layers of transistors. It has drawn attention as a promising alternative due to its relatively large bandgap (1.3–1.8 eV), high carrier mobility (~200 cm^2/V s range at room temperature),[6,7] and absence of dangling bonds.[7] Note that bulk MoS_2 has n-type semiconducting characteristics with an indirect bandgap (~1.3 eV),[8] whereas single-layer MoS_2 has a direct bandgap (~1.8 eV).[9] However, to realize the high performance MoS_2 transistors, not only own material characteristics but also the transport mechanism should be investigated. For example, a previous study reported that the electron mobility of single-layer MoS_2 field-effect transistors (FETs) in an air/MoS_2/SiO_2 structure was too low (0.5–3 cm^2/V s) for many applications.[10] However, when the carrier transport mechanism was considered, single-layer MoS_2 FETs using high-k HfO_2 as a dielectric layer for top gates have demonstrated electron mobilities over 200 cm^2/V s and high on/off ratios (~10^8) by suppressing Coulomb scattering.[7]

A few early reports suggest that multilayer MoS_2 surpasses single-layer MoS_2 in FET applications because it has a larger density of states and helps to create a larger channel carrier density, which boosts the current drive of FETs made using this system[11] and also has better noise immunity in air.[12] Moreover, multilayer MoS_2 is more well-suited for practical fabrication process to form large area as well. Unfortunately, for these multilayer MoS_2 FETs, the carrier transport mechanism and molecule absorption effects, critically related to transistor performances, has not yet been intensively explored for use in electronics at realistic operating temperatures (the working temperatures of commercial displays rise to +50 °C, and the extended temperatures increase to +85 °C). Even though a few reports have studied on temperature-dependent characteristics, such as the effective Schottky barrier height, these papers only focused on the single- or bi-layer MoS_2 FETs below room temperature.[13–15] In addition, except for multilayer MoS_2, it is well known that absorbed molecules on surfaces result in the degradation of the performances of single- or bi-layer MoS_2 transistors.[16,17]

Therefore, in this paper we report observed preliminary evidence of the dominant scattering mechanism and the temperature dependent performance of multilayer MoS_2 thin film transistors (TFTs). From the measurements of the temperature-dependent conduction at practical working

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temperatures (from room temperature up to 350 K), extracted drop-off rates of the mobility are helpful knowledge to use as the active channel materials of the thermistors. Also, to show the effect of operating ambient on the devices, we specifically investigated the electrical characteristics in the linear regime (at low drain voltage, V_D) as a function of operating temperatures in air and in a vacuum ($\sim 10^{-5}$ Torr). It exhibits that the multilayer MoS_2 transistors are more stable and less sensitive to ambient, comparing to the very thin single-layer MoS_2 transistors.

Fig. 1(a) shows a schematic architectural diagram for a fabricated multilayer MoS_2 FET. A SiO_2 dielectric layer with a thickness of 300 nm was deposited by chemical vapor deposition (CVD) on a heavily doped p-type Si wafer (resistivity $< 5 \times 10^{-3}\,\Omega$ cm). Multilayer MoS_2 flakes ($\sim$50 nm) were mechanically exfoliated from bulk MoS_2 crystals (SPI Supplies, USA), and transferred onto the deposited SiO_2 layer. For the source and drain electrodes, Ti (10 nm) and Au (300 nm) were deposited by electron-beam evaporation and were patterned by conventional UV photolithography and lift-off techniques. Ti ($\sim$4.3 eV) was selected among the low work function materials because it has been suggested as a good contact for injection into the conduction band of MoS_2.[9] Furthermore, Ti has been suggested since it is a transition metal with *d* orbitals that blend constructively with Mo4*d* states. Therefore, this favorable interface geometry is expected to facilitate good bonding and allow maximized injection at the contacts by increasing the overlap between the states at the interface.[9] Lastly, for reducing the contact resistance and residue, fabricated devices were treated by thermal anneal process at 200 °C in a vacuum furnace for 2 h with 100 sccm Ar and 10 sccm H_2. Fig. 1(b) shows a 3-dimensional (3D) confocal laser microscope (LEXT OLS4000, Olympus) image of a fabricated multilayer MoS_2 FET with the bottom gate structure. Measurements using an atomic force microscope showed that the thickness of the MoS_2 channels was around 50 nm among the measured devices shown in Fig. 1(b). Fig. 1(c) shows the drain current versus drain voltage (I_D-V_D) curves for representative multilayer MoS_2 TFTs with a channel length of 4 μm and width of 5 μm, as a function of V_D in a range from 0 to 30 V with the selected gate voltage (V_G) ranging from −70 to +70 V in steps of 35 V. The fabricated multilayer MoS_2 TFTs exhibited conventional n-type behavior with negative threshold voltages (V_{TH}). An on/min current ratio (I_{on}/I_{min}) of $\sim 10^7$ and a sub-threshold slope (SS) of 3.4 V/decade were obtained and the field effect mobility in the saturation regime ($\mu_{eff\_sat} \approx 10.9\,cm^2/V\,s$ extracted at $V_G = -25$ V, V_G-$V_{TH} < V_D$) was evaluated from a linear fitting of the curve of $I_D^{0.5}$ versus V_G at a fixed high source-drain voltage ($V_D = 30.0$ V) as shown in Fig. 1(d). Initially, our device exhibited the square-law behavior at low V_G (−40 V to −15 V), well. However, the device shown saturated I_D for V_G above −15 V, even though V_D did not reach V_G-V_{TH}. This notes that other authors have proposed that this strong saturation in output characteristics can partially be explained by the self-heating effect (corresponding to the intermediate regime) before reaching the negative I_D-V_D slope regime (where the self-heating effect is dominant).[18]

To further our understanding of the carrier transport mechanisms in multilayer MoS_2 TFTs, we investigated the effect of the ambient conditions (in air and in a vacuum) in combination with the variable operating temperature measurements. The transfer curves, I_D-V_G, were obtained in the linear regime (at a low V_{DS} of 0.1 V) to create a uniform charge density in the accumulation layer and the field effect mobility in the linear regime ($\mu_{eff\_lin} \approx 14.0\,cm^2/V\,s$) was calculated at room temperature by the MOSFET square-law model

$$\mu_{eff} = \frac{dI_D}{dV_G} C_i \times \frac{1}{V_D}, \tag{1}$$

where C_i is the insulator capacitance per unit area. We note that Das and others suggested that the maximum potential of back-gated multilayer MoS_2 TFTs with the thickness in the range of 30–60 nm and Scandium (Sc) contacts would be

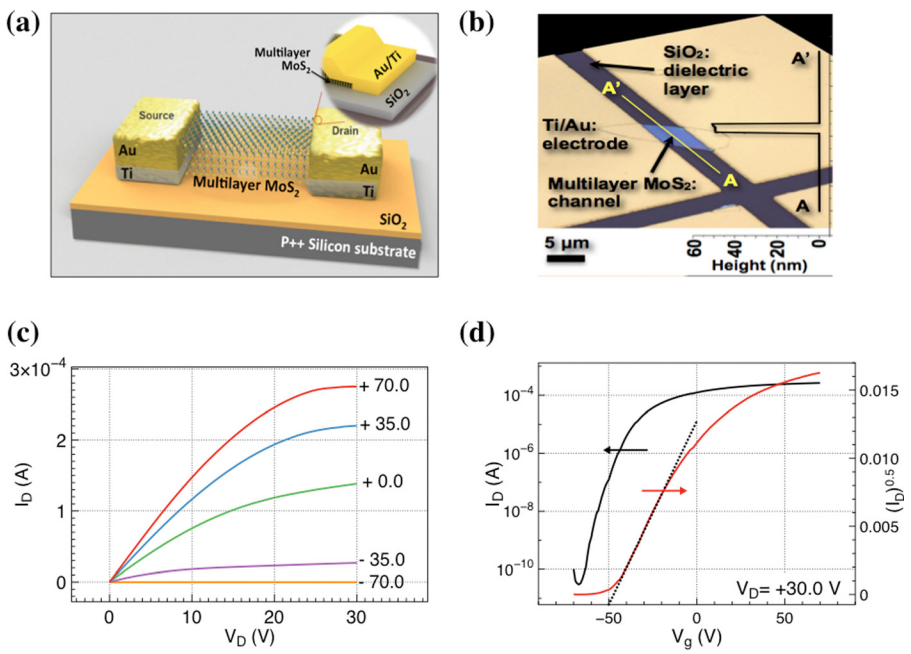

FIG. 1. Multilayer MoS_2 FET structure and its representative characteristics at room temperature: (a) the cross-sectional schematic structure of a multilayer MoS_2 FET with a 300-nm-thick SiO_2 gate dielectric; (b) the top view of a 3D confocal laser microscope image of a multilayer MoS_2 transistor after fabrication; (c) the plot of I_D-V_D; and (d) plots of I_D-V_G (left axis) and $I_D^{0.5}$-V_G (right axis).

limited around 50 $cm^2/V\,s$ due to involving interlayer coupling resistances.[19] Therefore, the extracted μ_{eff} both in saturation and linear regimes are lower than that of reported results, but nevertheless we can boost the μ_{eff} through the metals with lower work function (like Sc (3.5 eV)) than Ti (4.3 eV)/Au (5.1 eV) for reducing the Schottky barrier and through a high-k dielectric layer for minimizing the effect on Coulomb electron scattering. Priority, the contact resistance factor should be well separated from measured extrinsic characteristics to explicate the transport mechanism inside the MoS_2 semiconductor channel. Here, the Y function method (YFM) was hired to extract the intrinsic low field mobility (μ_0, the maximum available mobility in this system) and contact resistance (R_c)[20,22,23]

$$Y = \frac{I_D}{\sqrt{G_m}} = \sqrt{\frac{W}{L} C_i \mu_0 V_D} \times (V_G - V_{TH}), \tag{2}$$

where C_i is the insulator capacitance per unit area. The μ_0 can be extracted from the slope of Y function (Fig. 3(b), discussion later in detail). Note that the slope of the plot is 1.45×10^{-4} as shown in Fig. 2(a) and the extracted μ_0 at a low V_{DS} of 0.1 V is 14.6 $cm^2/V\,s$. If the contact effect is dominant, the extracted μ_{eff_lin} should be significantly lower than μ_0 and the non-linear I_D-V_D curves should be presented at low V_D as well. However, μ_0 (14.6 $cm^2/V\,s$) was only 3% more than the extrinsic μ_{eff_lin} (14.0 $cm^2/V\,s$) at the same V_D. Furthermore, the linear I_D-V_D curves were presented clearly at low V_D. Another interesting aspect is that the extracted μ_{eff_lin} (14.0 $cm^2/V\,s$) is higher than μ_{eff_sat} (10.9 $cm^2/V\,s$). First, this may originate from the fringing effect and/or the scattering effect. The fringing currents depend on V_D, the 1:1 aspect ratio of the channel would overestimate the calculated μ_{eff}, particularly when the MoS_2 flakes exceed the contacted channel width. Second, it is well known that the μ_{eff_sat} is commonly less affected by the contact resistance than μ_{eff_lin}. Therefore, the μ_{eff_lin} should be lower than μ_{eff_sat} in contact resistant dominant system. To investigate this phenomenon more specific, the R_{c_max} (23.4 kΩ) was estimated from the mobility attenuation factor ($\theta = \mu_0 C_i R_c W/L$).[22,23] θ can be extracted by following equation:[20,22]

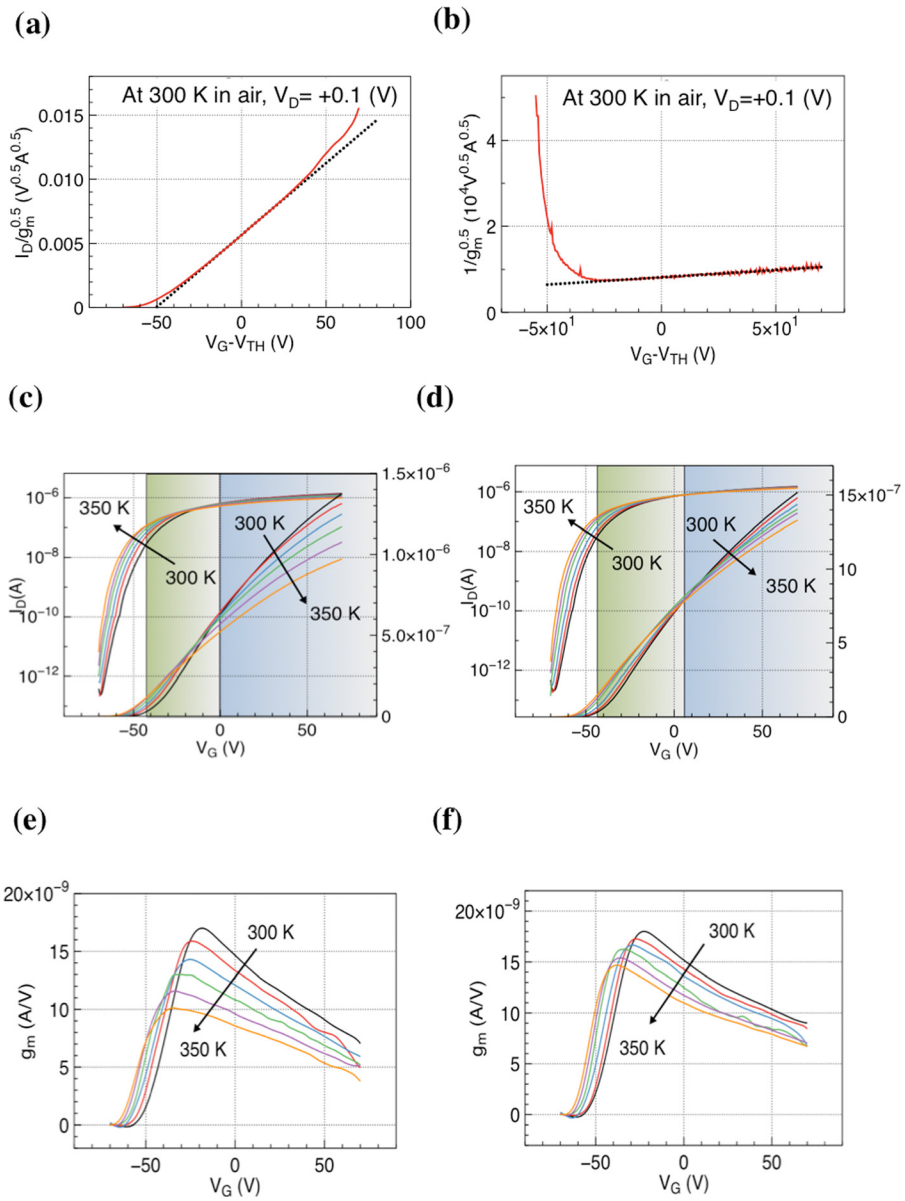

FIG. 2. (a) The $I_d/g_m^{0.5}$ plot with linear fitting in ambient condition, (b) the plot of $1/g_m^{1/2}$ with respect to gate voltage with linear fitting for evaluation of mobility attenuation factor, θ, (c) the typical I_D-V_G transfer characteristics of the fabricated multilayer MoS_2 transistor at V_{DS} of 0.1 V in air and (d) in a vacuum at different operating temperatures (T = 300, 310, 320, 330, 340, and 350 K) in both log and linear scales, and (e) transconductance versus V_G curves in air and (f) in a vacuum at different operating temperatures.

$$g_m = \frac{\partial I_D}{\partial V_G}, \quad (V_D = \text{const}) = \frac{W}{L} C_i \frac{\mu_0}{[1+\theta(V_G - V_{TH})]^2} \times V_D. \tag{3}$$

From Eq. (3), we can know that the θ can be calculated from the slope of the plot ($1/g_m^{1/2}$ versus V_G) and the linear fitted slope is 33.16 as shown in Fig. 2(b). Also, to calculate the channel resistance (R_{ch}) and to compare with R_{c_max}, the total resistance ($R_{total} = R_c + R_{ch}$) was calculated from I_D-V_D curves at low V_D and the obtained R_{total} and R_{ch} were 333.4 kΩ and 310 kΩ, respectively. For double-checking the value of R_{ch}, we directly calculated from induced charge carriers, $R_{ch} = L/(\mu_0 W C_i (V_G - V_{TH}))$ once again. Note that the reconfirmed R_{ch} was ~250 kΩ and both values of R_{ch} are larger than R_c in this system. Therefore, it can be possible that the effect of scattering is more significant than the effect of contact resistance.[24] We address these features in more depth later with the transconductance (G_m) and the $\mu \sim T^r$ law, specifically.

To describe the electrical characteristics for the variable operating temperatures, two regimes (green and blue regions) based on the zero temperature coefficient (ZTC) point in the on-state were defined in Figs. 2(c) and 2(d). At the ZTC gate voltage, the devices exhibit constant DC performance with operating temperature. However, the fabricated TFTs did not show a clear ZTC point. Thus, the minimum point of dI/dT was set as a cut-off point to divide the two regimes. Qiu and others reported that a Schottky barrier was formed between the Ti/Au metal contact and the MoS_2 semiconductor in their research; the structure investigated was the same as our structure. Their Schottky barrier height was ~65 meV, which exceeded the thermal emission energy at room temperature.[25] Therefore, at low V_G (below V_{TH}), these barriers partially hindered the flow of carriers. However, when the operating temperature increased, the carriers easily overcame these barriers by thermionic emission.[26] This caused I_{min} to rise.

Figs. 2(e) and 2(f) show that the G_m decreased at high V_G in this device, regardless of measured temperatures. Such G_m decrease might be due to dominant R_c and/or phonon scattering.[20,21] As V_G increases, the influence of the injection barriers can be reduced, then it has become decreasing the temperature dependence. However, G_m rolled off at high V_G (blue region) as shown in Figs. 2(e) and 2(f). As discussed in previous paragraph, the scattering effect, which is inversely proportional to the operating temperatures and at high field was having much effect on our system. To confirm the phonon scattering impact on performances, the output characteristics were investigated as a function of temperatures. Phonon scattering dominated by the $\mu \sim T^r$ law has two different types of phonon scattering corresponding to the exponent parameter (r): acoustic phonon scattering ($-1 < r < 0$) and optical phonon scattering ($r < -1$). In our device, the extracted r values in air and in a vacuum are −3.5 and −1.7, respectively. Therefore, we posit that optical phonon scattering is dominant in these systems, similar to other observations.[11,27] Furthermore, at low V_G and above V_{TH} (green region), the drain current seems to be slightly increased due to the dominant negative V_{TH} shift, as shown in Figs. 2(c) and 2(d) as a function of the operating temperature. The combination of increased I_{min} by thermionic emission and reduced I_{on} by phonon scattering contributes to the decreased I_{on}/I_{min} ratio.

The estimated SS, V_{TH}, μ_{eff_lin}, and μ_o were plotted in Figs. 3(a) and 3(b), respectively, corresponding to different temperatures and ambient. The estimated SSs are relatively larger than those of the conventional metal oxide FETs due to interface trap density between semiconductor and insulator layers. In addition, aforementioned Schottky barriers (at low V_G, below V_{TH}) can lead a relatively large SS originated from the tunneling through a barrier.[28] Regardless of the ambient, the SS values are almost same. Even though the thickness of multilayer MoS_2 is around 50 nm, the actual channel is few layers near the bottom. This is why the thicker multilayer MoS_2 TFTs showed less effects of ambient conditions on interface quality as determined by SS values.[12,29]

Temperature dependent characteristics of V_{TH} are exhibited in Fig. 3(a). V_{TH} shifts toward the negative direction as the temperature increases. This behavior is observed in most semiconductor systems due to an increase in thermally generated carriers, resulting in a shift in the Fermi level in the semiconductor. The average rate of shift reached −0.32 V/K (300–350 K) regardless of the ambient conditions. Additionally, V_{TH} was higher in air than in a vacuum. One possible explanation is that the oxygen and water molecules on the surface of MoS_2 semiconductors could be adsorbed from the ambient air,[13,16,30] and they could trap the charge carriers from the conduction band. This could make depleted channels and induce a positive V_{TH} shift.[30] Larger mobility drop-off rate in air (0.12 cm^2/V s K), comparing to the mobility drop-off rate in vacuum (0.07 cm^2/V s K) was exhibited. The phonon scattering limited mobility have been shown the temperature and the effective electric field dependency.[31] The adsorbed oxygen and water molecules might be attributed to the increased effective electric field

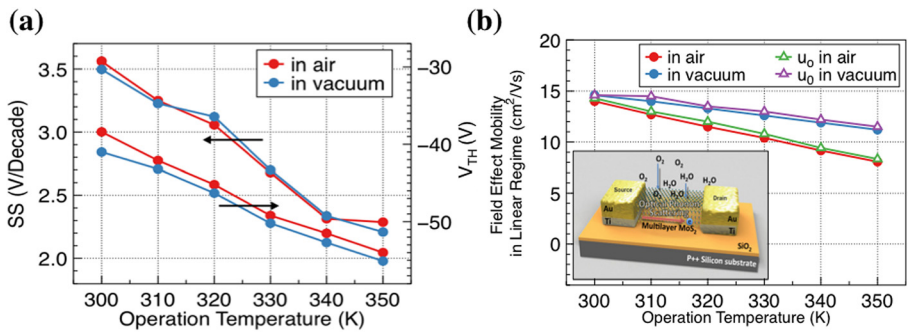

FIG. 3. The operating temperature dependence of the sub-threshold slope (SS), threshold voltage (V_{TH}), and field effect mobility in the linear regime (μ_{eff_lin}) and intrinsic mobility (μ_0 at V_{DS} of 0.1 V) (a) in air and (b) in a vacuum at different operating temperatures.

and phonon mode, confirmed by the increased exponent parameter (r). On the other hand, the μ_0 extracted from Y-function shows almost identical values, comparing to extrinsic mobility and drop-off rates, regardless of the operation temperatures in Fig. 3(b). It can interpret that the transport mechanism of this system can be the phonon scattering of MoS_2 channel, not limited by the contact resistance. Furthermore, the ratio ($\mu_{eff\_lin\_vacuum}/\mu_{eff\_lin\_air}$) is ~0.95 at 300 K. This is higher than the previously reported values.[13,16,30] This observation is consistent with the fact that the impact of absorbed oxygen and water molecules on the fabricated device performance is weaker than that for thinner MoS_2 layers, because the impact of attached molecules on a semiconductor surface in a bottom-gated device is normally related to the surface to volume ratio.[32]

In conclusion, the electrical characteristics of the multilayer MoS_2 transistors at real operating temperatures (from room temperature to 350 K) were shown, and the impact of ambient conditions on device performance was revealed. By comparing μ_{eff} of the transistors with increasing operating temperatures, we determined that μ_{eff} was limited by phonon scattering at high operating temperatures and was augmented by thermionic emission at low gate voltages, thus reducing I_{on}/I_{min}. The decreasing rate of μ_{eff} corresponding to the increased operating temperatures was larger in air than in a vacuum due to surface scattering and trap sites caused by chemisorption. In addition, at room temperature, ambient conditions had little influence on the current density and μ_{eff} of multilayer MoS_2 channels compared to those of single or thinner MoS_2-based transistors. This is because the multilayer MoS_2 had a smaller surface to volume ratio, thus limiting the effect of surface states on the transport in the underlying channel.

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