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Letter

Flexible nano-hybrid inverter based on inkjet-printed organic and 2D multilayer MoS_2 thin film transistor

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ABSTRACT

We report a novel platform on which we design a flexible high-performance complementary metal–oxide–semiconductor (CMOS) inverter based on an inkjet-printed polymer PMOS and a two-dimensional (2D) multilayer molybdenum disulfide (MoS_2) NMOS on a flexible substrate. The initial implementation of a hybrid complementary inverter, comprised of 2D MoS_2 NMOS and polymer PMOS on a flexible substrate, demonstrates a compelling new pathway to practical logic gates for digital circuits, achieving extremely low power consumption with low sub-1 nA leakage currents, high performance with a voltage gain of 35 at 12 V supply voltage, and high noise margin (larger than 3 V at 12 V supply voltage) with low processing costs. These results suggest that inkjet-printed organic thin film transistors and 2D multilayer semiconducting transistors may form the basis for potential future high performance and large area flexible integrated circuitry applications.

1. Introduction

The growing demands for high performance, human-centric electronics have been the driving force for advances in flexible semiconductors and novel processing strategies. Advances in materials, including inkjet-printed organics [1,2], 1-dimensional semiconductors (single-walled carbon nanotubes, nanowires, etc.) [3,4] and two-dimensional (2D) layered semiconductors (graphene, transition metal chalcogenides) [5,6] have contributed to the development of flexible switching/driving transistors and have generated human-centric soft electronics including epidermal electronics [7], flexible displays [8], artificial organs [9], and biomedical devices [10]. Due to this interest, various semiconducting thin-film transistors (TFTs) and device structures have been proposed to integrate them into digital circuitry building blocks such as inverters, logic gates, and ring oscillators [1,2,4].

However, these TFT channel materials are inherently complex to dope as *n*- or *p*-channel and implementing a complementary metal–oxide–semiconductor (CMOS) inverter is technically more difficult because both of the *p*- and *n*-channel transistors should be patterned together on a common substrate. One simple alternative, as published in previous reports is to exploit a pseudo-inverter, which consists of unipolar transistors and an enhancement load using different work-function gate electrodes.

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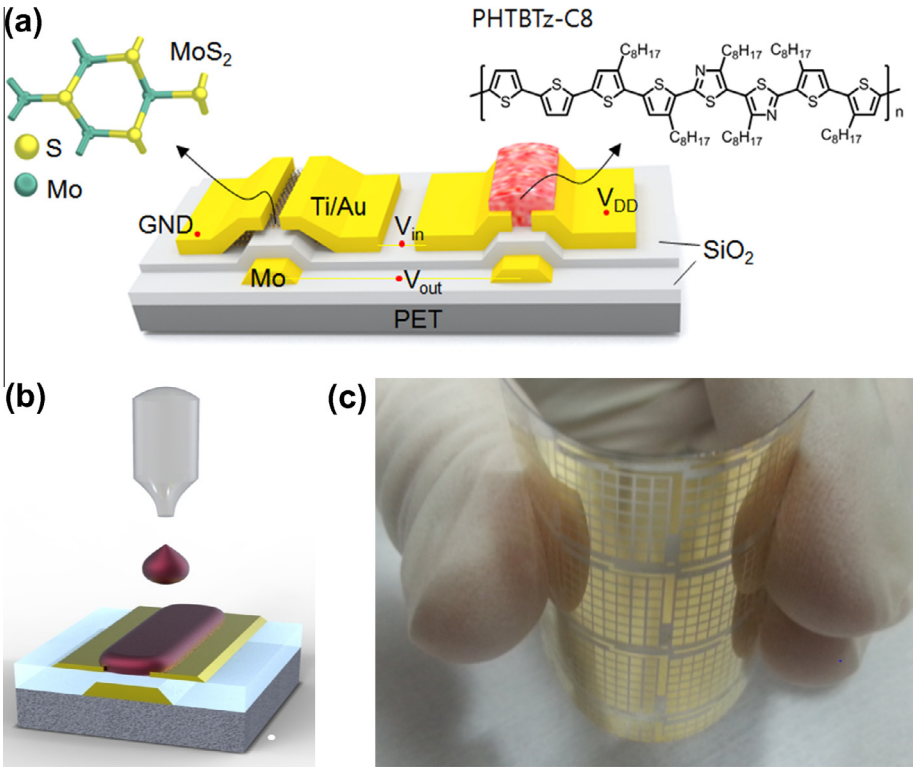

Fig. 1. (a) Schematic structure of our hybrid complementary inverter with MoS_2 (n-type) and PHTBTz-C8 (p-type) channels. Insets: schematic chemical structures of MoS_2 and PHTBTz-C8. (b) Inkjet printing scheme of PHTBTz-C8 PMOS. (c) Photograph of flexible hybrid inverter on a thin sheet of PET film.

Generally, logic gates that are composed of complementary transistors have both pull-up networks (PUNs) which are constructed with *p*-channel transistors and pull-down network (PDN) with *n*-channel transistors. Since PUNs provide a conditional connection from V_{DD} to the output node, and PDNs provide one from GND to the output the complementary logic gates generally offers better functional robustness (larger noise margin), faster propagation delay, and lower power consumption. In the case of pseudo-logic building blocks based on unipolar (only *p*-channel or *n*-channel), transistor based logic gates, the PDN or PUN is replaced with a load device, which results in significant degradation of noise margin, unbalanced propagation delay, and increasing power consumption due to the short circuit current.

For the realization of high performance, low power digital circuit building blocks on the flexible substrates, the key challenge is to exploit optimal semiconductors that can simultaneously offer low temperature processing, mechanical flexibility, and a feasible process of integrating individual devices into large-scale integrated circuits [9]. Here, we report a novel platform on which we design a comparatively high-performance complementary inverter based on an inkjet-printed polymer PMOS and a 2D layered molybdenum disulfide (MoS_2) NMOS on a flexible substrate [11]. Inkjet printing allows the deposition of uniformly patterned *p*-type poly (tetryloctylhexathiophene-alt-dioctylbithiazole) (PHTBTz-C8) polymer into specific active channels by selectively 'dropping' small amounts of polymer inks onto specific locations to form device patterns [2]. Reliable and uniform polymer PMOS in these integrated inverters has excellent properties: a mobility as high as 0.25 cm^2/Vs [12], the small device-to-device performance variation, and large-area scalable integration up to nearly on 4″ or 6″ sized plastic substrates. Furthermore, 2D layered semiconductors (series of transition metal dichalcogenides (TMDs) with the formula MX_2, where M = Mo, W and X = S, Se, etc.) are also considered to be the most attractive *n*-channel materials for flexible and stretchable electronics. Previous reports demonstrate that MoS_2 TFTs exhibits exceptional characteristics; mechanical reliability of 2D layered crystals, relatively large bandgaps (1.2–1.9 eV), high mobilities at room temperature (up to ~500 cm^2/Vs), a low subthreshold swing (*SS*, ~70 mV/decade), high on/off ratios (~10^7), and amenability to low-cost, large-area growth technique such as chemical vapor deposition (CVD) [13–15]. Though large-area CVD growth of 2D MoS_2 remains unaddressed in this work, the initial implementation of a hybrid complementary inverter, comprised of 2D MoS_2 NMOS and polymer PMOS on a flexible substrate, demonstrates a compelling new pathway to practical logic gates for digital circuits, achieving extremely low power consumption with low sub-1 nA leakage currents, high performance with a voltage gain of 35 at 12 V supply voltage, and high noise margin (larger than 3 V at 12 V supply voltage) with low processing costs.

2. Experimental

Fig. 1a shows a schematic structure of our hybrid complementary inverter with MoS_2 NMOS and PHTBTz-C8 PMOS on a flexible polyethylene terephthalate (PET) substrate. NMOS and PMOS have bottom gate/top contact and bottom gate/bottom contact configuration, respectively. In order to fabricate individually addressed local bottom gate electrodes, sputtered molybdenum layer was patterned by using photolithography and etching. Silicon dioxide (SiO_2) with a thickness of 300 nm was deposited by plasma-enhanced (PE) CVD as gate insulator. Then, thin flakes of 2D layered MoS_2, peeled off from bulk crystals by micromechanical exfoliation, was transferred onto the SiO_2 gate insulator. The thickness of a MoS_2 flake is statistically observed as being 30 ± 20 nm. The source and drain electrodes (Ti/Au) were deposited through e-beam evaporation, and patterned by a lift-off process. After fabricating NMOS device based on MoS_2, the surface of gate insulator was treated with self-assembled monolayers (SAM) of octadecyltrichlorosilane (ODTS) (purchased from Aldrich) for enhancing TFT performances. Polymer semiconducting material (PHTBTz-C8) was dissolved in tetrahydronaphthalene (THN) at a concentration of 0.2 wt%, and then printed onto as-fabricated source/drain electrodes using Dimatrix inkjet-printer in atmosphere, as shown in Fig. 1b. Samples were annealed at 160 °C for 1 h in an N_2 environment.

The transfer characteristics (drain current I_{DS} vs. gate-source voltage V_{GS} at two different drain-source voltage V_{DS}) and output characteristics (I_{DS} vs. V_{DS} at multiple constant V_{GS}) are measured using an Keithley 4200-SCS Semiconductor Analyzer connected to a probe station.

3. Results and discussion

Before characterizing the novel hybrid complementary inverter, the electrical transport properties of the *n*- and *p*-type TFT devices are first investigated individually. First, the *n*-type characteristics of the MoS_2 TFT are presented in Fig. 2. The inset of Fig. 2 also shows an optical microscope image of as-fabricated MoS_2 TFT (gate length: $L = 9.2$ μm and width: $W = 11.5$ μm) with a 300-nm-thick SiO_2 gate insulator. MoS_2 crystals are expected to provide *n*-channel characteristics with low threshold voltage because their conduction band edge is near the Fermi level of the Ti/Au electrode. By contrast, the PHTBTz-C8 channel based OTFTs exhibit *p*-type behavior, thereby achieving efficient hybrid complementary inverter by obtaining symmetrical transfer curves. In a transfer (I_{DS}–V_{GS}) curve of the MoS_2 TFT (see Fig. 2a), typical transistor characteristics are observed with an on-off current ratio (I_{on}/I_{off}) of $\sim 1 \times 10^6$, a threshold voltage (V_T) of 1.7 V and a subthreshold swing ($SS = dV_{GS}/d\log I_{DS}$) of 2.65 V decade^{-1} at low drain voltage ($V_{DS} = 1$ V). Here, the V_T is estimated from the plot of the square root of the drain current vs. gate voltage ($\sqrt{I_{DS}} - V_{GS}$). In the linear regime, a field-effect mobility (μ_{eff}) of 42 cm^2/Vs is extracted by $\mu_{eff} = Lg_m/(WC_{ox}V_{DS})$, where g_m is the maximum transconductance and C_{ox} is the gate oxide capacitance. Desirably, our *n*-channel TFT offers a high μ_{eff} value due to the high electron mobility of multilayer MoS_2 crystals, as shown in Fig. 2c. The output curves (I_{DS}–V_{DS}) show the good modulation with the variation of gate biases from 0 to 15 V with a 3 V step (ΔV_{GS}). At a low V_{DS}, the MoS_2 TFT shows a linear output curve and the saturation regime is also clearly observed at high V_{DS} due to the pinch-off, which agrees well with other conventional long-channel transistors (see Fig. 2b).

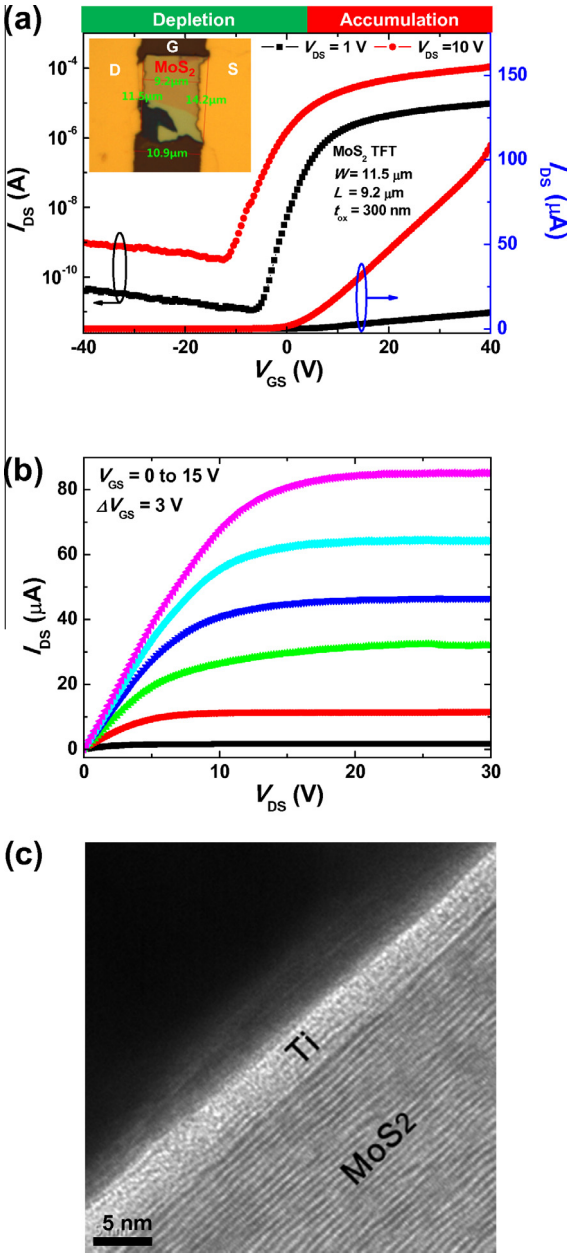

Fig. 2. (a) Transfer characteristics (I_{DS}–V_{GS}) of n-type MoS_2 measured at two different drain voltages of 1 V and 10 V. Inset: optical microscope image of fabricated MoS_2 TFT (gate length: $L = 9.2$ μm and width: $W = 11.5$ μm). (b) Output characteristics (I_{DS}–V_{DS}) of the same MoS_2 TFT. (c) Cross-section transmission electron microscopy image of multi-layered MoS_2 flake.

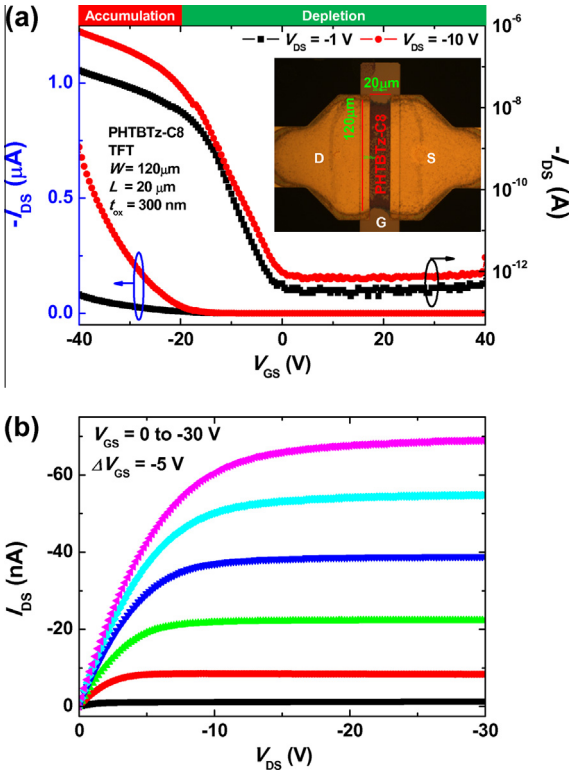

Fig. 3. (a) Transfer characteristics (I_{DS}–V_{GS}) of p-type TFT with PHTBTz-C8 measured at two different drain voltages of 1 V and 10 V. Inset: optical microscope image of fabricated PHTBTz-C8 TFT (gate length: L = 20 μm and width: W = 120 μm). (b) Output characteristics (I_{DS}–V_{DS}) of the same TFT.

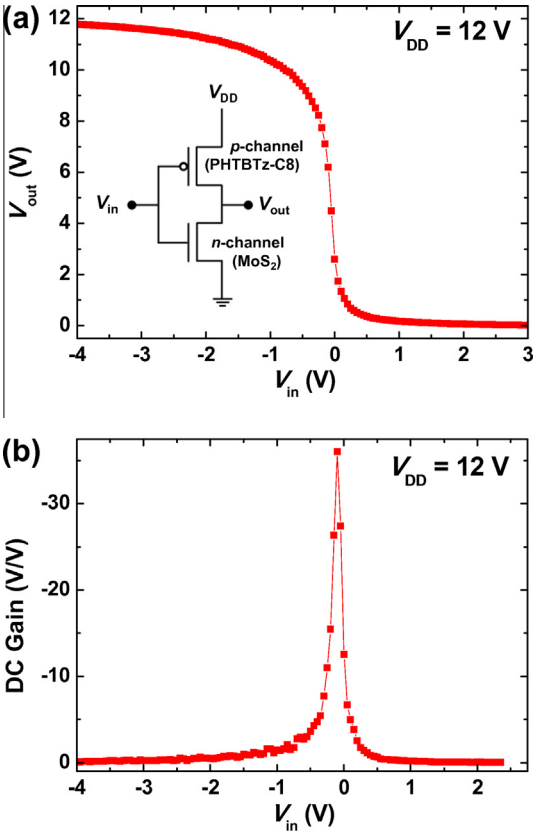

Fig. 4. (a) Voltage transfer characteristic curves of the hybrid complementary inverter with MoS_2 (n-type) and PHTBTz-C8 (p-type) channels. Inset: equivalent circuit diagram of the hybrid complementary inverter. (b) Signal gain of the same device.

Fig. 3 shows the transfer and output characteristic curves of *p*-type OTFT with a polymer semiconductor channel. The inset of Fig. 3a shows an optical microscope image of the fabricated polymer semiconductor transistor. The polymer presented herein consists of a copolymer based on thiophene and thiazole, where the thiophene acts as electron-donating unit and the thiazole is the electron-accepting one. The presence of a thiazole unit within the molecular backbone is anticipated to stabilize the highest occupied molecular orbital (HOMO) level, and planarize the molecules backbone, thus enhancing the intra-molecular charge transfer leading to high charge carrier mobility [16–18]. In general, the molecular packing and microstructure in organic thin films greatly affect the semiconducting performance of these films. According to our previous report, PHTBTz-C8 can be readily self-assembled into highly ordered lamellar structures in the thin films, owing to the strong intermolecular interaction force contributed from the π–π stacking, donor–acceptor interaction, and intermolecular side-chain lengths [12]. Therefore, this polymer semiconductor shows good film-forming nature and electrical performance fabricated by inkjet printing technique. Note that the polymer semiconductor ink can be directly deposited on selected areas of substrate by an inkjet printing process, which leads to efficient fabrication yield for the hybrid complementary inverter. The inkjet-printed PHTBHz-C8 polymer semiconductor-based OTFTs have a standard channel width of 120 μm and a channel length of 20 μm. As shown in Fig. 3a, the PHTBTz-C8 OTFT also exhibits the typical *p*-channel transfer characteristics. In a given range of V_{GS}, the I_{DS} initially increased linearly and then saturates at larger negative values of V_{GS} with the I_{on}/I_{off} of ~1.9×10^6, V_T of −10.7 V, *SS* of 2.89 V/decade and μ_{eff} of 0.24 cm^2/Vs at V_{DS} = −1 V. When the V_{GS} is swept from 0 V to −30 V with a −5 V step of ΔV_{GS} (see Fig. 3b), the output curves also exhibit a good modulation with both a linear triode regime and a saturation regime.

Based on the electrical transport properties presented in Figs. 2 and 3, the performance of our proposed organic-inorganic hybrid CMOS inverter with *n*-channel MoS_2 device and *p*-channel PHTBTz-C8 OTFT device is characterized. Fig. 4 shows the static voltage transfer characteristics (V_{TC}) and respective gains of noble hybrid CMOS inverter as a function of supply voltage (V_{DD}) of 12 V. As shown in Fig. 4, the noise margin of the high input level (NM_H) is approximately 4 V and that of the low input level (NM_L) is over 3 V, which are sufficient to guarantee the robust functionality of the inverter. Fig. 4b also shows that the voltage gain (dV_{out}/dV_{in}) increases with supply voltage V_{DD}, and reaching up to 35 at a 12 V supply voltage. The large noise margin and the gain of the inverters demonstrates that the proposed CMOS inverter is applicable to real digital circuits and/or standard cell implementations.

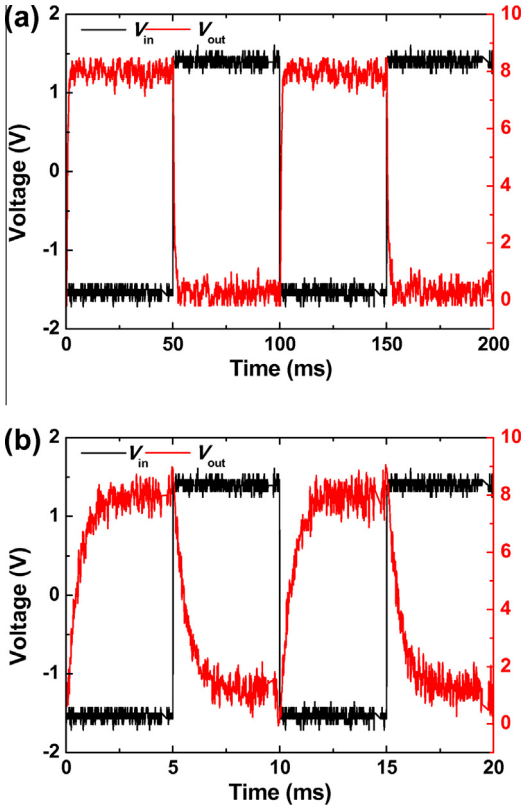

Fig. 5. Dynamic switching characteristics of the hybrid complementary inverter with MoS_2 (n-type) and PHTBTz-C8 (p-type) channels at (a) 10 Hz and (b) 100 Hz input signals.

The dynamic behaviors of the inverter are measured and the results are shown in Fig. 5. The proposed inverter has a rail-to-rail output with 10 Hz and 100 Hz square wave inputs. In the rising transition, the output node of the inverter is charged through the *p*-channel PHTBTz-C8 OTFT device, while the output node is discharged through *n*-channel MoS_2 device in the falling transition. From the measurements, the rising time (t_r) and falling time (t_f) are obtained to be 1.39 ms and 1.81 ms, respectively. The rising time (t_r) means the time taken for the output node to be charged from 10% of V_{DD} voltage level to 90% V_{DD}, and the falling time (t_f) is the time for the output to be discharged from 90% V_{DD} to 10% level. The low to high delay (T_{PLH}), which means the propagation delay from the input falling to 50% level of V_{DD} to the output rising to 50% of V_{DD}, is measured to be 370 μs, and the high to low delay (T_{PHL}) that means the propagation delay in the opposite direction is 462 μs. Since the inverter's transition time is the time interval during which the output capacitance is charged or discharged, delay parameters such as rising time, falling time and transition delay can be reduced with smaller output node capacitance.

4. Conclusion

In conclusion, we have demonstrated high performance mechanically flexible complementary inverters made up of 2D layered MoS_2 TFTs and inkjet-printed polymer OTFTs. Due to the highly flexible properties of both materials, all individual transistors can potentially be integrated into unit blocks for switching/driving components and will be developed into practical logic gates for digital circuits on flexible substrates. In particular, the extremely low sub-1 nA leakage current, unlike the popular unipolar thin-film inverter, may drive the development of these hybrid CMOS inverters. These results suggest that inkjet-printed OTFTs and 2D layered semiconducting transistors may form the basis for potential future high performance and large area flexible integrated circuitry applications.

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