Electrical Contact Analysis of Multilayer MoS_2 Transistor With Molybdenum Source/Drain Electrodes

Geonwook Yoo, Sungho Lee, Byoungwook Yoo, Chuljong Han, Sunkook Kim, and Min Suk Oh

***Abstract*— We demonstrate a two-dimensional (2D) multi-layered molybdenum disulfide (MoS_2) transistor with molybdenum (Mo) side and edge contacts, which is deposited using a dc-sputtering method. It exhibits field-effect mobility of 23.9 cm^2/Vs and ON/OFF ratio of 10^6 in a linear region. A current–voltage study under different temperatures (300–393 K) reveals that the Mo–MoS_2 transistor shows a band transport characteristics, and a Schottky barrier height of 0.14 eV is estimated using a thermionic emission theory. Finally, the side and edge contacts of Mo–MoS_2 are confirmed through the transmission electron microscope analysis. Our results not only show that Mo can be an alternative contact metal to other low work-function metals but also that the edge contact may play an important role in resolving the performance degradation over thickness increase of the MoS_2 channel layer.**

***Index Terms*— Molybdenum, edge contact, Schottky barrier, contact resistance, MoS_2.**

I. INTRODUCTION

TWO-DIMENSIONAL (2D) materials such as molybdenum disulfide (MoS_2) have drawn great interests as promising channel materials for emerging electronic devices [1]–[5]. MoS_2 has a relatively large band gap (1.2 - 1.8 eV) depending on a number of layers [1], a high mobility (~200 $cm^2/V \cdot s$) with a high-k dielectric layer [2], and absence of dangling bonds [3]. Moreover, its atomically thin 2D layered structure is suitable for a thin-film transistor (TFT) structure, and therefore MoS_2 can have an advantage of relatively simple fabrication process steps for large area low-cost electronics [4]. These unique properties have been facilitating intensive research efforts to i) understand the electrical [3], [4] and optical [6], [7] properties, ii) find proper contact metals [8], [9], interface layers [10], and diverse applications [4]–[6].

Especially, metal contacts to MoS_2 have been investigated intensively since it is one of major factors limiting device performance. Its large band gap and lack of controllable as well as stable doping methods result in a Schottky contact instead of an ohmic contact at the metal-MoS_2 interface [9]. Therefore several researches have focused on reducing a Schottky barrier height and contact resistance by adopting not only low work-function metals such as Sc (3.5 eV) [8], In (4.1 eV) and Ti (4.3 eV) [11] but also other 2D materials (e.g. graphene) [9]. Ti in particular is a high-performance contact attributed to its metallization of MoS_2 layer by forming Ti-S covalent bonds [11]. However, those low work-function metals may suffer from poor surface stability and thermal/electrical conductivity. Although Mo is not a low-work function metal (4.5 eV), it is one of the elements of MoS_2 and induces metallization of MoS_2 layer under the contact, resulting in reduced tunnel barrier and therefore improvement to Mo-MoS_2 contact properties. Recently, Mo is explored as an alternative contact to monolayer and few layer MoS_2 using simulations and experiments [12].

In this letter, we present electrical contact analysis of multilayer MoS_2 transistor with DC-sputtered Mo S/D contacts in more detail. We investigate electrical properties and temperature-dependence of Mo-MoS_2 transistor from I-V measurements for 300 K ~ 393 K. A Schottky barrier height (Φ_{SB}) is extracted, and other contact properties are also studied. Finally, possibility of edge contact formation in addition to side contact is verified using transmission electron microscope (TEM) analysis, and its contribution to the electrical characteristics is discussed.

II. EXPERIMENTS

Multilayered MoS_2 flakes were mechanically exfoliated from bulk MoS_2 crystals (Graphene market, USA) by a conventional scotch-tape method, and then transferred to a heavily doped p-type Si substrate with thermally grown 200 nm SiO_2 layer. S/D contacts were patterned on top of MoS_2 flakes using conventional lift-off technique. Mo (120 nm) was deposited by DC magnetron sputtering with 150 W in argon (Ar) ambient. The fabricated device was then annealed at 573 K in N_2 for 10 min using a rapid thermal annealing to remove any absorbed organic residues and to improve contact resistance. The thickness of the MoS_2 channel layer and other TFT dimensions (W/L) were identified using atomic force microscope (AFM) and an optical microscope, respectively. Current-voltage (I-V) measurements from 300 K to 393 K were performed by using a semiconductor parameter analyzer (HP 4156C) and a probe station with a temperature controlled

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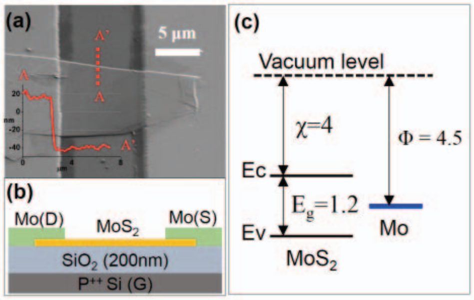

Fig. 1. (a) SEM image of the fabricated MoS$_2$ transistor with Mo S/D contacts (Inset) AFM profile of the MoS$_2$ channel thickness. (b) Cross sectional schematic of Mo-MoS$_2$ transistor with side and edge contact. (c) Band alignment of MoS$_2$ with Mo.

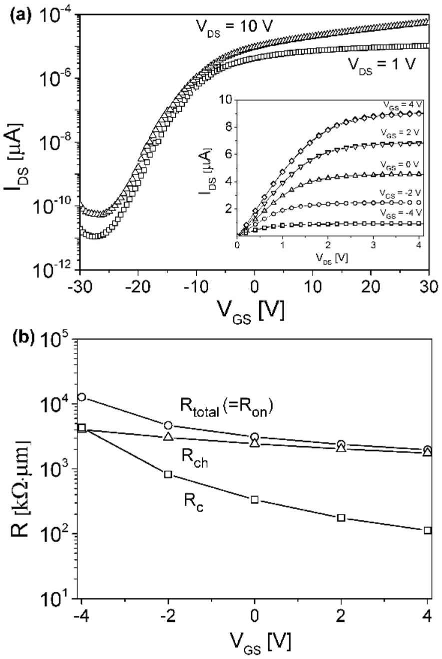

Fig. 2. (a) Transfer characteristics of the Mo-MoS$_2$ TFT for V_{DS} = 1 V and 10 V. (Inset) Output characteristics for $V_{GS} = -4, -2, 0, 2, 4$ V. (b) Extracted total resistance (R_{total}), calculated channel (R_{ch}) and contact resistance (R_c) as a function of gate voltage. R_c takes ~6 % of R_{total}.

chuck (MSTECH M6VC). To observe side and edge contacts to multilayer MoS$_2$, a sample was prepared and analyzed by using focused ion-beam (FIB) -SEM and TEM (JEOL, JEM-2100F), respectively.

III. RESULTS AND DISCUSSIONS

Fig. 1(a) and (b) show an SEM image and cross-sectional schematic of the fabricated MoS$_2$ transistor, respectively. In the inset of Fig. 1(a), we identify the MoS$_2$ channel layer was ~ 67 nm thick using AFM, which is corresponding to ~ 96 MoS$_2$ monolayers and bulk-like bandgap of 1.2 eV. The band diagram in Fig. 1(c) represents a work-function alignment of Mo (4.5 eV) contact to a multilayered MoS$_2$.

TABLE I

SUMMARY OF CONTACT RESISTANCE FOR DIFFERENT CONTACT METALS

Metal	MoS$_2$ layer	L [µm]	C$_{OX}$ [F/cm^2]	V$_{GS}$-V$_{TH}$ [V]	R$_C$ [kΩ·µm]	Ref.
Ti	46	3	3.8e-8 (SiO$_2$)	~57	~53	[13]
Ni	7	0.5	1.1e-8 (SiO$_2$)	~20	~200	[14]
Mo	4	2	9.1e-8 (Al$_2$O$_3$)	~65	~2	[12]
Mo	96	10	1.7e-8 (SiO$_2$)	~14.1	~112	This work

Fig. 2 (a) shows the measured transfer curves of I_{DS}-V_{GS} for V_{DS} = 1 and 10 V, and output curves of I_{DS}-V_{DS} for $V_{GS} = -4, -2, 0, 2, 4$ V. The field-effect mobility (μ_{FE}) of 23.9 cm^2/Vs in a linear operation region was extracted from $\mu_{FE} = L \cdot g_m/(W \cdot C_{OX} \cdot V_{DS})$, where $W/L = 10.1\mu$m/10 μm, $C_{OX} = 1.7 \times 10^{-8}$ F/cm^2, V_{DS} = 1 V. The on/off-current ratio (I_{ON}/I_{OFF}) of ~ 10^6 and sub-threshold swing (*SS*) of 2.47 V/dec were also obtained, and threshold voltage (V_{TH}) was calculated to be −10.1 V by using linear extrapolation method in a linear region (V_{DS} = 1 V). V_{TH} was found from the intercept of a tangent at the max. g_m with V_{GS} axis.

Fig. 2(b) shows the extracted on-state resistance (R_{on}) in a linear region from the I_{DS}-V_{DS} curves, and channel resistance (R_{ch}), which is calculated from $R_{ch} = L/(\mu_{FE} \cdot W \cdot C_{OX} \cdot (V_{GS} - V_{TH})$ where W/L, C_{OX}, μ_{FE}, and V_{TH} values are from a linear region, is also presented. Resistance value was normalized with the channel width. Based on the extracted R_{on} and the calculated R_{ch}, Mo-MoS$_2$ contact resistance (R_c) was obtained from $R_{on} = R_{ch} + 2 \cdot R_c$, and a value of ~112 kΩ · μm is found at V_{GS} = 4 V. It is slightly higher or similar with that of Ti and Ni contact to multilayer MoS$_2$ measured even under very high gate-bias from the recent works as summarized in Table I. Although it is ~50 times higher than that of same Mo contact to 4-layer MoS$_2$ at a very high overdrive voltage (V_{GS} - V_{TH}), the difference is mainly attributed to the gate-bias condition since edge-contact between Mo and multilayer MoS$_2$ is achieved in our case and thus MoS$_2$ interlayer effect is minimized [12].

By performing I-V measurements for different temperatures (300 - 393 K), we obtained temperature-dependence of Mo-MoS$_2$ transistor and estimated Φ_{SB}. Fig. 3 (a) shows the transfer characteristics shift with increasing temperatures, and the inset represents temperature-dependent behaviors of μ_{FE} and V_{TH}. μ_{FE} and V_{TH} were extracted in the same manner as described above. μ_{FE} decreases from 24.0 to 16.6 cm^2/V · s as the temperature increases; V_{TH} shifts toward a negative direction from −10.1 to −20.1 V. The decrease of μ_{FE} is due to surface roughness and phonon scattering in the channel instead of Mo-MoS$_2$ contact, and the negative shift of V_{TH} is caused by thermally generated charges in the channel. These trends are band transport characteristics with the Mo-MoS$_2$ contacts [13].

Next, we built Arrhenius plot based on Fig. 3 (a), and by assuming conventional thermionic emission theory, we extracted Φ_{SB} from the equation $J_{DS} = A^* \cdot T^2 \cdot exp(-q\Phi_B/kT) \cdot [exp(qV_{DS}/kT) - 1]$, where A^* is Richardson constant, T is temperature, q is the elementary charge, k is the Boltzman constant [8]. In Fig. 3 (b), effective Φ_{SB} of 0.14 eV is extracted at

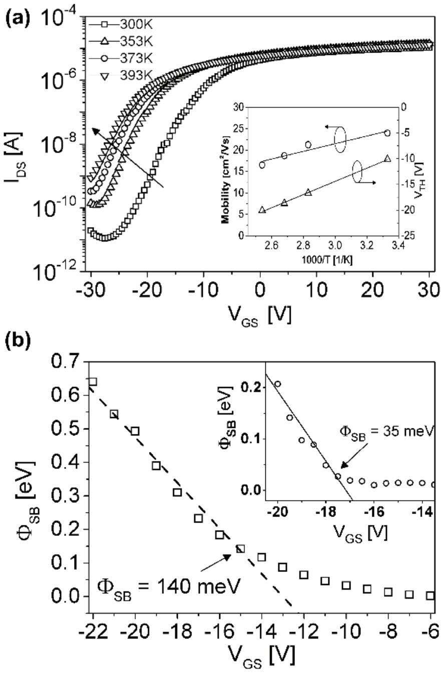

Fig. 3. (a) $I_{DS} - V_{GS}$ transfer curves at $V_{DS} = 1$ V for 300 – 393 K. (Inset) The temperature-dependence of the field-effect mobility (μ_{FE}) and threshold voltage (V_{TH}). (b) Extracted Schottky barrier height (Φ_{SB}) as a function of gate-bias (V_{GS}) (Inset) Extracted Φ_{SB} with no V_{TH} shift.

a specific bias, and this value is similar with $\Phi_{SB} = 0.1$ eV that is calculated by density functional theory simulation [12]. Since the Φ_{SB} could be overestimated in the presence of large V_{TH} shift in our experiment, compensated Φ_{SB} (35 meV) was also extracted by shifting I-V curves for temperatures higher than 300 K as shown in the inset of Fig. 3 (b). This significant reduction of Φ_{SB} was because the current component in off-states due to V_{TH} shift was excluded and therefore I_{DS} was much lowered.

Since S/D electrodes cannot contact all the layers and gate-bias can modulate bottom layers only, μ_{FE}, R_c, and I_{DS} properties degrade exponentially with the thickness of MoS$_2$ in absence of edge contacts [8], [13]. Thus edge contacts are important in multilayer MoS$_2$ to enhance electrical performance by taking advantage of contacting all the conducting channels. Our Mo-MoS$_2$ transistor (96L) shows similar or slightly worse electrical properties compared to few-layer (3L - 5L) MoS$_2$ with Mo side contact which was measured even under high vacuum as summarized in Table II, and this improvement can be explained with edge contact formed by conformal deposition of DC-sputtering. Fig. 4 shows TEM images with energy dispersive spectroscopy (EDS) analysis from the side and edge contact; transition layer at the interface of side and edge contact was 1.55 ~ 1.92 nm thick, in which atomic % ratio of Mo:S changed roughly from 35:65 (MoS$_2$) to 90:10 (Mo). The transition layer formed due to interface mixing effect by high energy deposition of DC-sputtering method used in this work. Role of edge contact, which was proved in graphene experimentally and theoretically [16], [17], has been proposed in multilayer MoS$_2$ case theoretically [8], [11], [12]. In this work, we believe that the edge contact might contribute to maintain electrical performance in thick multilayer MoS$_2$ transistor compared to that of side contacted few-layer MoS$_2$ case. Further experimental studies for various MoS$_2$ thicknesses and other contact metals are suggested to corroborate the edge contact effect in general.

TABLE II
COMPARISON OF FIELD-EFFECT MOBILITIES FOR DIFFERENT MoS$_2$ THICKNESS

MoS$_2$ layer	W/L	C_{OX} [F/cm^2]	Measurement condition	μ_{FE} [cm^2/Vs]	Ref.
1	2/2	9.1e-8 (Al$_2$O$_3$,72nm)	300K/ 1e-6 mbar	~13	[12]
3	-			~27	
4	3.8/2			~26	
96	10.1/ 10	1.7e-8 (SiO$_2$, 200nm)	300 K/ 1 atm	~24	This work

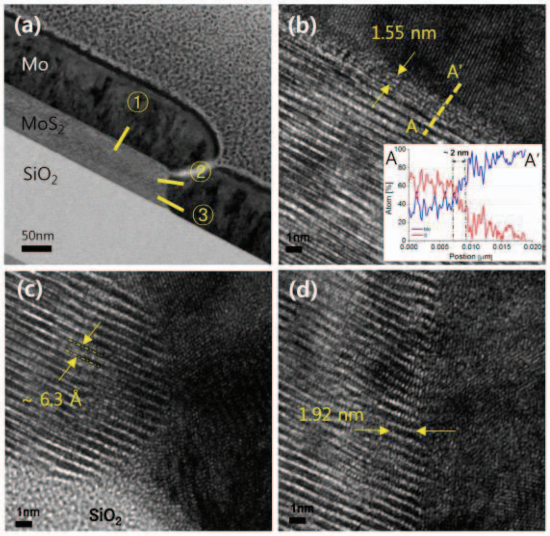

Fig. 4. (a) Cross sectional TEM image of Mo-MoS$_2$ contact with indications of measured locations. (b) Side contact from the top (①) showing transition layer thickness of 1.55 nm, which is estimated using EDS analysis (Inset). (c) Edge contact from the bottom (③) showing MoS$_2$ interlayer thickness of 0.63 nm. (d) Edge contact from the side (②) showing transition layer thickness of 1.92 nm.

IV. CONCLUSION

In summary, we have fabricated multilayer MoS$_2$ transistor with side and edge contacted Mo S/D electrodes which was deposited by DC sputtering. I-V characterizations under different temperatures showed a band transport characteristics, and a Schottky barrier height of 0.14 eV was estimated. The Mo-MoS$_2$ transistor displayed similar μ_{FE} (23.9 cm^2/Vs in linear regime) and, I_{DS} (~1 μA/μm at $V_{DS} = 1$ V, $V_{GS} = 30$ V) compared to previous optimal finite layer MoS$_2$ transistor with Mo side contact only. Our experimental results suggest that edge contact may play an important role in resolving performance degradation over thickness increase of MoS$_2$ channel layer.

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