AIP Applied Physics Letters

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Citation: Applied Physics Letters **107**, 201103 (2015); doi: 10.1063/1.4935979
View online: http://dx.doi.org/10.1063/1.4935979
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/107/20?ver=pdfcov
Published by the AIP Publishing

APPLIED PHYSICS LETTERS **107**, 201103 (2015)

Photosensitivity enhancement in hydrogenated amorphous silicon thin-film phototransistors with gate underlap

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(Received 26 August 2015; accepted 3 November 2015; published online 16 November 2015)

Conventional ɑ-Si:H phototransistors exhibit poor photosensitivity due to low photo-conversion efficiency. To overcome this intrinsic limit, we introduce gate underlap in ɑ-Si:H phototransistors and demonstrate photosensitivity enhancement. We show that photocurrent can be significantly larger than dark current by 4 orders of magnitude, using 1-μm gate underlap at incident optical power density (P_{inc}) of 3.2 W/cm^2. Our 1-μm gate-underlap phototransistor exhibits higher photosensitivity than the device without gate underlap by 64 times with $P_{inc} = 0.2$ W/cm^2 and a wavelength of 785 nm. Our gate-underlapped phototransistors also show excellent time-resolved photoswitching behaviors, demonstrating the great potential for highly sensitive photodetectors.
 [http://dx.doi.org/10.1063/1.4935979]

Since the concept of ubiquitous computing was outlined by Mark Weiser, interactive display technologies have been widely explored.[1] The interactive display plays a great role in the ubiquitous computing system that can carry out real-time interaction between humans and digital devices by sensing user's motion or touch.[2] An infrared (IR) photosensor composed of photodiode or phototransistor array might be most suitable for actual applications because it can easily detect user's motion with or without physical contact and map into images from the input signals.[3–5] Some important properties required for photosensors are low cost, high sensitivity, and the integration of sensors into active matrix display backplane. In this regard, hydrogenated amorphous silicon (ɑ-Si:H) based devices have been considered and adopted as a strong candidate for various photosensor applications due to the favorable properties for the requirements mentioned above.[6–8] However, the ɑ-Si:H leads to low photo-conversion (photon to excess carriers) efficiency, which intrinsically limits its use for high-sensitivity photodetectors having a large signal-to-noise ratio.[9] In this work, we demonstrate significant enhancement of photosensitivity in ɑ-Si:H phototransistors based on the novel gate-underlapped structure that we have previously developed for the layered-semiconductor thin-film transistors (TFTs) where the photoresponsivity of indirect-bandgap multilayer MoS_2 phototransistor was significantly enhanced by 3 orders of magnitude as compared to a device without gate underlap.[10,11] The geometrical effects on electrical and optical properties with different lengths of ungated region (gate underlap) will be discussed in detail. By introducing gate underlap, electrical properties such as mobility and on/off current ratio (I_{on}/I_{off}) are degraded accordingly, but it can significantly enhance the photosensitivity of ɑ-Si:H device. Finally, time-resolved photoresponse measurement is performed to evaluate photoswitching capability of our gate-underlapped ɑ-Si:H TFT.

Figures 1(a) and 1(b) show a 2D cross-section view and an optical micrograph of the fabricated ɑ-Si:H TFT with gate underlap on a glass substrate. The gate length is shorter than the channel length due to the ungated channel (gate underlap) region. A 200-nm-thick Cr gate electrode was deposited on the substrate by sputtering and it forms a bottom-gate geometry. A tri-layer comprising SiN_x gate insulator (400 nm), ɑ-Si:H active layer (170 nm, the doping concentration of 10^{16} cm^{-3}), and n$^+$ ɑ-Si:H layer (70 nm, the doping concentration of 10^{19}–10^{20} cm^{-3}) was deposited without vacuum break by plasma-enhanced chemical vapor deposition (PECVD).[12] An electron-beam evaporated Ti/Au (20/200 nm) was used as source/drain (S/D) electrodes. After patterning the S/D electrodes, back channel etch (BCE) technique was conducted to remove the n$^+$ ɑ-SiH in the back channel region. All patterning process was performed by standard photolithography, dry and wet etching. To investigate the effect of the different device geometry, the gate underlap lengths (L') of 0 μm, 1 μm and 2 μm were used without changing the channel length ($L = 10\ \mu$m) and the width ($W = 15\ \mu$m). Electrical measurements of the ɑ-Si:H TFTs were performed using a semiconductor characterization system (Keithley 4200 SCS) at room temperature in atmospheric environments.

Figure 2(a), which is transfer characteristics of ɑ-Si:H TFTs with and without gate underlap at drain voltage (V_{ds}) of 1 V, exhibits the significant suppression of on current as L' increases. The field-effect mobilities (μ_{eff}) of the 0-μm, 1-μm, and 2-μm gate-underlap TFTs were extracted to be 0.29, 0.05, and 0.02 cm^2/V s, respectively. This can be understood from the fact that the gate modulation is inefficient in the ungated region of the bottom-gate TFTs and the gate underlap behaves like a series resistor both at the source and

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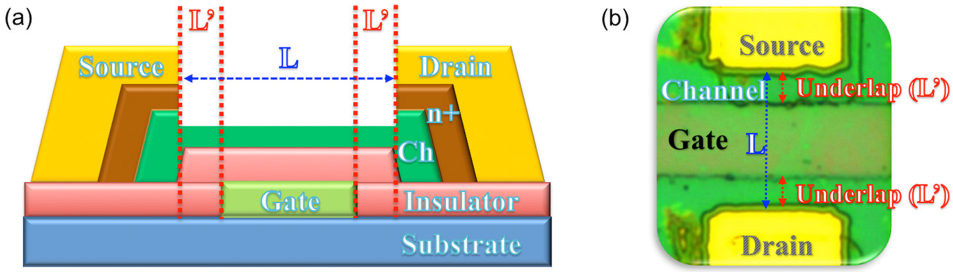

FIG. 1. (a) 2D cross-sectional schematic of a bottom-gate α-Si:H TFT with gate underlap. The dashed lines indicate the length of gate underlap (L'). (b) Optical microscope image in top view of the fabricated α-Si:H TFT.

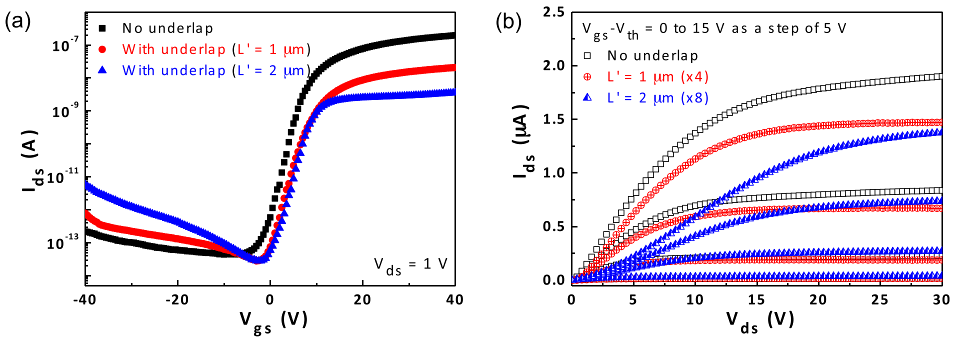

FIG. 2. (a) Transfer characteristics of the bottom-gate α-Si:H TFTs at $V_{ds} = 1$ V with various gate underlap lengths. (b) Output characteristics of the same phototransistors. The current level was adjusted for 1-μm and 2-μm gate underlap devices for the sake of discussion and comparison.

the drain sides.[11] Other performance metrics of transistors such as on-off current ratio (I_{on}/I_{off}) and subthreshold swing (SS) are also gradually degraded with the gate underlap. Figure 2(b) compares the output characteristics (I_{ds}–V_{ds}) of the α-Si:H TFTs. For the sake of discussion, we adjusted the current level of two gate-underlapped TFTs in Fig. 2(b) to compare the device characteristics properly. It clearly shows that, as the gate underlap increases, non-linear behavior becomes more significant as usually observed in Schottky-barrier field-effect transistors, which indicates the weak interconnection of channel with the source/drain contacts through the large gate underlap.

Next, we investigated optoelectronic properties of the bottom-gate α-Si:H TFTs with gate underlap and compared against the device without gate underlap. We measured the transfer characteristics repeatedly at various incident optical power densities of 0.2, 0.4, 0.8, 1.6, and 3.2 W/cm^2 with a fixed wavelength of 785 nm (near IR) as well as under a dark condition. Figures 3(a)–3(c) show the transfer characteristics of the α-Si:H TFTs without gate underlap and with 1-μm and 2-μm gate underlap, respectively. In all cases, under the incident light, electron-hole pairs are generated in the channel region, and the excess carriers increase the total current of the device. The increase in the current by comparison with the dark current is photocurrent (I_{ph}) induced by photo illumination, which is directly affected by the optical power density of the incident light as shown in Fig. 3. In the presence of gate underlap, holes can be accumulated in the bottom-gate region, which reduces the potential barrier for electrons, boosting thermionic current further.[11] Consequently, as the length of gate underlap increases, the difference between the total current under illumination (I_{total}) and the dark current (I_{dark}) increases, particularly at the on state, as presented in Figs. 3(b) and 3(c).

To understand the role of gate underlap, we have measured I_{ds}–V_{ds} characteristics of a floating gate α-Si:H TFT (using the structure without gate underlap), which can be regarded as a two-terminal resistor, under illumination with various incident optical power densities. First, Fig. 4(a) shows symmetry with respect to the origin at $V_{ds} = 0$ V, which clearly indicates that the quality of contacts in our device is controlled perfectly during the fabrication process and the source and the drain have the same level of contact quality. Second, as we can see in Fig. 4(a), the total current increases dramatically under illumination. We have also plotted resistance as a function of incident optical power

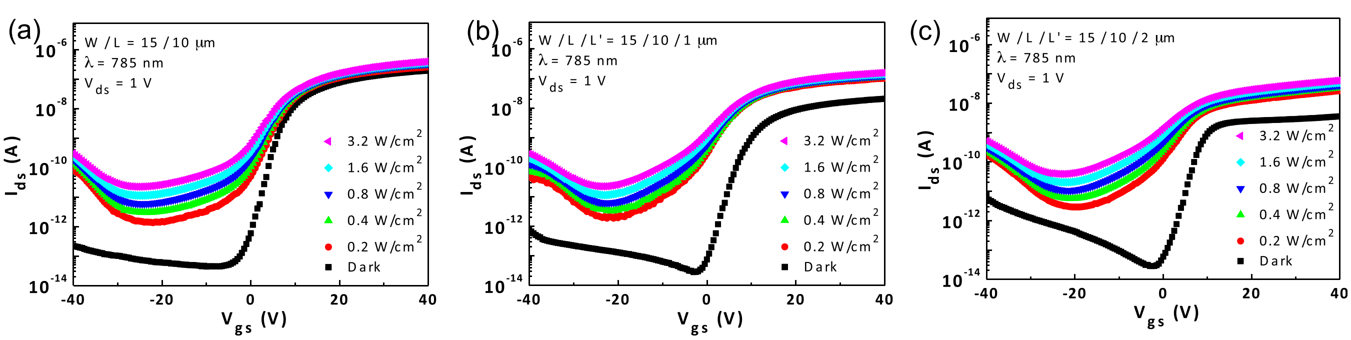

FIG. 3. Transfer curves under illumination at various incident optical power densities for α-Si:H phototransistors (a) without gate underlap ($L' = 0\,\mu$m), and with gate underlap of (b) $L' = 1\,\mu$m and (c) $L' = 2\,\mu$m at $V_{ds} = 1$ V. Wavelength of the laser is 785 nm and incident optical power densities are 0, 0.2, 0.4, 0.8, 1.6, and 3.2 W/cm^2.

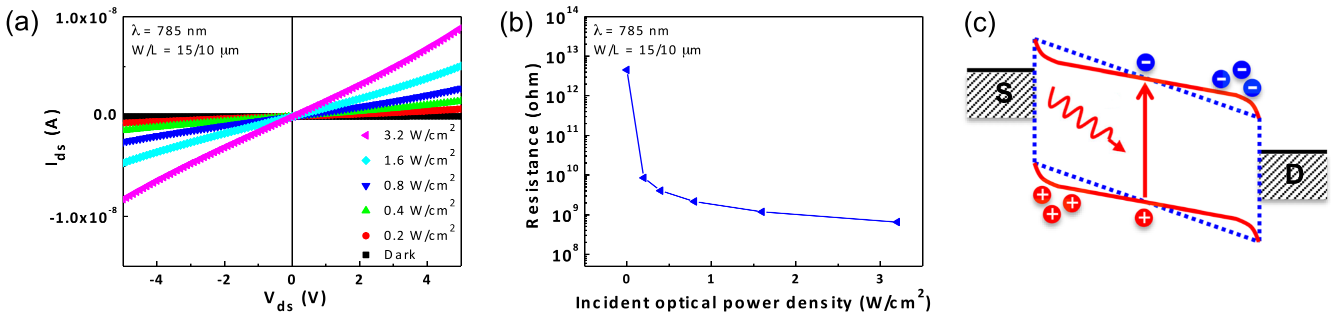

FIG. 4. (a) I_{ds}–V_{ds} curves for a floating gate α-Si:H TFT without gate underlap at the dark state and under illumination at various light power densities of 0.2, 0.4, 0.8, 1.6, and 3.2 W/cm^2 with the laser wavelength of 785 nm. (b) Resistance as a function of incident optical power density. (c) Band diagram under illumination (red solid lines) at $V_{ds} > 0$. Blue dotted lines show conduction and valence bands at the dark state.

density in Fig. 4(b), which shows that the resistance reduces significantly even with very weak incident optical power density, i.e., by ~3 orders of magnitude at 0.2 W/cm^2 as compared to the dark state. This can be attributed to Schottky barrier thinning at the contact-channel interface as shown in Fig. 4(c). Carriers generated during the illumination are accumulated at the interface (electrons at the drain side, and holes at the source side when a positive V_{ds} is applied), which lower potential barrier height, resulting in thinner Schottky barrier and significantly lager carrier injection from the contact to the channel. As the incident optical power density increases, the resistance reduces even further, but it is saturated to a certain value as shown in Fig. 4(b), where the resistance does not decrease linearly with the increase in the incident optical power density since the increased number of electrons injected from the source due to the barrier thinning, in turn, increases the potential barrier by a certain amount, making the increase of power density (increasing the number of photons and electron-hole pairs) less effective in reducing the contact resistance, particularly at high optical power densities.

In order to quantify the effect of photo-illumination for various gate underlap lengths in the bottom-gate α-Si:H TFTs, we have plotted the sensitivity as a function of gate underlap length for different light power density in Fig. 5(a). Photosensitivity (S) or signal-to-noise ratio, which provides the practical figure-of-merit for photodetectors, can be defined as[13,14]

$$S\,(\%) = \frac{signal}{noise} = \frac{I_{total} - I_{dark}}{I_{dark}} \times 100 = \frac{I_{ph}}{I_{dark}} \times 100. \qquad (1)$$

In general, the photosensitivity calculated based on the measurement data (Fig. 3) exhibits an increasing behavior with the length of gate underlap. Furthermore, the increase rate of sensitivity is drastically higher at larger incident optical power densities as shown in Fig. 5(a). Consequently, the photocurrent can be larger than the dark current by 4 orders of magnitude with 1-μm gate underlap at 3.2 W/cm^2 of light power density. Sensitivity ratio of the device with 1-μm gate underlap to the device without gate underlap ($S_{L'=1\mu m}/S_{L'=0\mu m}$) at the incident optical power density of 0.2 W/cm^2 is shown in Fig. 5(b), which reaches its peak at V_{gs} of 1.5 V. At this point, the sensitivity of the 1-μm gate underlap phototransistor is larger than that of the device without gate underlap by 64-fold. In a real image application, the most valuable figure of merit for a phototransistor/photodetector is a linear dynamic range (LDR), defined as 20 × $\log_{10}(I_{ph}/I_{dark})$, to identify the sensitivity of a photodetector. In this work, gate underlap leads to high photosensitivity (a large signal-to-noise ratio) as I_{dark} is significantly decreased while keeping the similar level of I_{ph}, and our relatively simple modification of phototransistor structure can greatly enhance the photosensing performance of α-Si:H phototransistors.

Finally, in order to characterize the photoswitching behavior of our α-Si:H TFTs with gate underlap, we measured time-resolved photoresponse of the α-Si:H TFT with $L' = 1\,\mu$m as shown in Fig. 5(c). The measurement was conducted at $V_{gs} = 0$ V and $V_{ds} = 10$ V with a 785-nm laser at different incident optical power densities (0.2, 0.4, 0.8, 1.6, and 3.2 W/cm^2). As the illuminating light was switched on and off with a period of 20 s, the photocurrent responded immediately. This excellent photoresponse near IR range demonstrates the practical potential application of α-Si:H phototransistors.

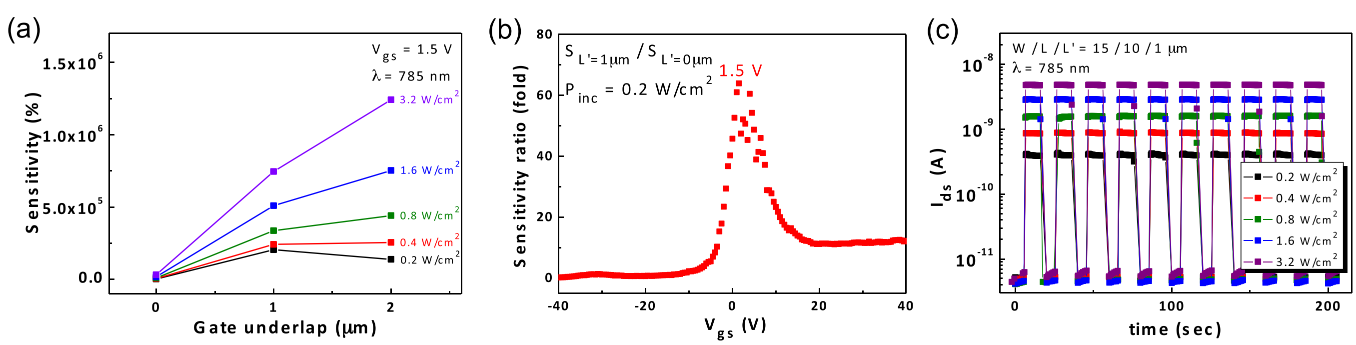

FIG. 5. (a) Extracted sensitivities from Fig. 3 as a function of gate underlap length for different incident optical power densities at $V_{gs} = 1.5$ V. (b) Sensitivity ratio of the device with gate underlap ($L' = 1\,\mu$m) to the device without gate underlap ($L' = 0\,\mu$m) at the incident optical power density of 0.2 W/cm^2. (c) Time-resolved photoswitching behavior of the gate-underlapped α-Si:H phototransistor ($L' = 1\,\mu$m). The incident laser was switched on and off at every 10 s.

In summary, we fabricated ɑ-Si:H thin-film phototransistors including gate-underlap region, and studied the electrical and optical characteristics by varying the length of gate underlap. Our gate-underlapped ɑ-Si:H phototransistor exhibited high sensitivity, which can be enhanced by 64 times as compared to the device without gate underlap. This huge photosensitivity and its excellent photoswitching behavior suggest that our bottom-gate ɑ-Si:H phototransistor with gate underlap can be a promising candidate of photodetectors for highly sensitive interactive displays as well as other large-area photosensor applications.

This work was supported in part by the National Research Foundation of Korea (2013M3C1A3059590, 2014M3A9D7070732, and 2013K1A3A1A32035549) and in part by NSERC Discovery Grant No. RGPIN-05920-2014.

[1]M. Weiser, Sci. Am. **265**, 94 (1991).
[2]S.-E. Ahn, I. Song, S. Jeon, Y. W. Jeon, Y. Kim, C. Kim, B. Ryu, J.-H. Lee, A. Nathan, S. Lee, G. T. Kim, and U.-I. Chung, Adv. Mater. **24**, 2631 (2012).
[3]S. Y. Han, D. C. Kim, B. Cho, K. S. Jeon, S. M. Seo, M. S. Seo, S.-W. Jung, K. Jeong, W. K. Kim, S.-H. Yang, N.-H. Kim, J. Song, H.-S. Kong, and H. G. Kim, J. Soc. Inf. Disp. **19**, 855 (2011).
[4]S. Y. Han, K. S. Jeon, B. Cho, M. S. Seo, J. Song, and H.-S. Kong, IEEE J. Quantum Electron. **48**, 952 (2012).
[5]S. Y. Han, K. T. Park, H. S. Jeon, Y. W. Heo, and B. S. Bae, J. Disp. Technol. **8**, 617 (2012).
[6]H.-S. Park, T.-J. Ha, Y. Hong, J.-H. Lee, B.-J. Lee, B.-H. You, N.-D. Kim, and M.-K. Han, J. Soc. Inf. Disp. **16**, 1165 (2008).
[7]G. Chaji, A. Nathan, and Q. Pankhurst, Appl. Phys. Lett. **93**, 203504 (2008).
[8]Y. Lee, I. Omkaram, J. Park, H.-S. Kim, K.-U. Kyung, W. Park, and S. Kim, IEEE Electron Device Lett. **36**, 41 (2015).
[9]J. M. Escalante and A. Martinez, Phys. B **407**, 2044 (2012).
[10]W. Choi, M. Y. Cho, A. Konar, J. H. Lee, G.-B. Cha, S. C. Hong, S. Kim, J. Kim, D. Jena, J. Joo, and S. Kim, Adv. Mater. **24**, 5832 (2012).
[11]J. Kwon, Y. K. Hong, G. Han, I. Omkaram, W. Choi, S. Kim, and Y. Yoon, Adv. Mater. **27**, 2224 (2015).
[12]Y. He, R. Hattori, and J. Kanicki, IEEE Electron Device Lett. **21**, 590 (2000).
[13]B. Yuan, X. J. Zheng, Y. Q. Chen, B. Yang, and T. Zhang, Solid State Electron. **55**, 49 (2011).
[14]Z. Pei, H.-C. Lai, J.-Y. Wang, W.-H. Chiang, and C.-H. Chen, IEEE Electron Device Lett. **36**, 44 (2015).