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Enhancement-mode operation of multilayer MoS_2 transistors with a fluoropolymer gate dielectric layer

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Enhancement-mode multilayer molybdenum disulfide (MoS_2) field-effect transistors (FETs), which are an immensely important component toward low-power electronics based on a two-dimensional layered semiconductor, are demonstrated using the fluoropolymer CYTOP as a gate dielectric. The fabricated devices exhibit threshold voltage (V_{TH}) of ~5.7 V with field-effect mobility (μ_{FE}) of up to 82.3 cm^2/V s, and the characteristics are compared with the depletion-mode characteristics of MoS_2 FETs with the cross-linked Poly(4-vinylphenol) gate dielectric ($V_{TH} \sim -7.8$ V). UV photoelectron spectroscopy analysis indicates that increased surface potential due to the surface dipole effect of the fluorine group influences the positive V_{TH} shift. *Published by AIP Publishing.*
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Molybdenum disulfide (MoS_2), a two-dimensional transition metal dichalcogenide, has drawn great interest as a promising transistor channel material for emerging electronic devices.[1–7] MoS_2 has a direct or indirect band gap (1.2–1.8 eV) depending on a number of layers,[8] a high mobility (~200 cm^2/V·s) with a high-k dielectric layer,[9] and absence of dangling bonds.[10] These unique properties have been facilitating intensive research efforts to address fundamental electrical and optical properties[10–12] and to investigate electrical contacts[13–15] and interface layers.[16,17] Furthermore, various basic and integrated electronic components for broad applications have been demonstrated based on mono- and multi-layered MoS_2 field-effect transistors (FETs).[4–7] Despite all the benefits, MoS_2 shows a very undesirable feature for highly integrated low-power circuits and systems; in many of the reported works,[10,12,14–17] MoS_2 FETs operate in a depletion-mode (i.e., a negative threshold voltage, V_{TH}). In other words, large negative gate-bias, not zero bias, must be applied in order to turn off the MoS_2 FETs since significant mobile carriers are already present in the channel even at a zero gate-bias condition. This feature requires a constant negative gate-bias to keep them off-state, resulting in a significant amount of power consumption as well as gate-bias stress effect. Therefore, an enhancement-mode operation (i.e., a positive V_{TH}) of MoS_2 FETs is of paramount importance to power-efficient circuits and low-power flexible electronics based on MoS_2.[18]

Although it has been recently reported that V_{TH} of MoS_2 FETs can be controlled by engineering the gate-metal work function,[4] treating sulfur vacancies,[19] and other approaches,[20–22] the tunable range of V_{TH} is rather small (<1 V) or the scheme itself is a highly elaborated method. An alternative approach can be a modulation of interface energy level by introducing additional self-assembled monolayers (SAMs), which contain a functional group on the molecular ends, at the interface between the semiconductor and gate dielectric.[23] The ultra-thin SAM layer with different functional groups would have different electron-withdrawing properties and, therefore, modulate the charge carrier density in the channel. CYTOP™, an amorphous fluoropolymer, is known to have strong hydrophobicity and electron-withdrawing property compared to Poly(4-vinylphenol) (PVP).[24,25] In this study, we demonstrate enhancement-mode multilayer MoS_2 FETs by adopting CYTOP as a gate dielectric, and compare their electrical characteristics with the same device structure except the Poly (4-vinylphenol) [PVP] dielectric. The electrical properties of the polymer thin-films as a gate dielectric are characterized by performing UV photoelectron spectroscopy (UPS) analysis and *C-V* measurement on a metal-insulator-metal (MIM) structure. Moreover, statistical variations of V_{TH}, subthreshold swing (*SS*) and field-effect mobility (μ_{FE}) are also compared and discussed, confirming the dielectric effects.

Figure 1 illustrated the fabricated multilayered MoS_2 FETs with the CYTOP and cross-linked PVP gate dielectrics. The chrome (Cr) glass with a Cr thickness of 90 nm was used as a back-gate electrode. Two polymer gate dielectrics were formed onto the Cr/glass as follows: (i) Poly-vinyl phenol (PVP) and poly(melamine-co-formaldehyde) [PMF], which is a cross-linking agent (1:1 mole ratio), were dissolved in propylene glycol methyl ether acetate [PGMEA] solvent (~10% wt.). Then the PVP gate dielectric layer was formed by spin-coating the solution at 3000 rpm for 60 s, followed by cross-linking for 30 min at 150 °C. (ii) CYTOP (3M, CTX-SP2) gate dielectric was formed simply by spin-coating a commercial product (3M, SP2) at 1500 rpm for 60 s, followed by curing at 70 °C for 30 min and baking at 180 °C for 60 min. The chemical structures of PVP and CYTOP are presented on the right-hand side of Fig. 1. Following the gate dielectric formation, mechanically exfoliated MoS_2 flakes from bulk MoS_2 crystals (Graphene market, USA) by a conventional scotch-tape method were transferred onto the polymer gate dielectrics. The atomic force microscopy (AFM) profile of the MoS_2

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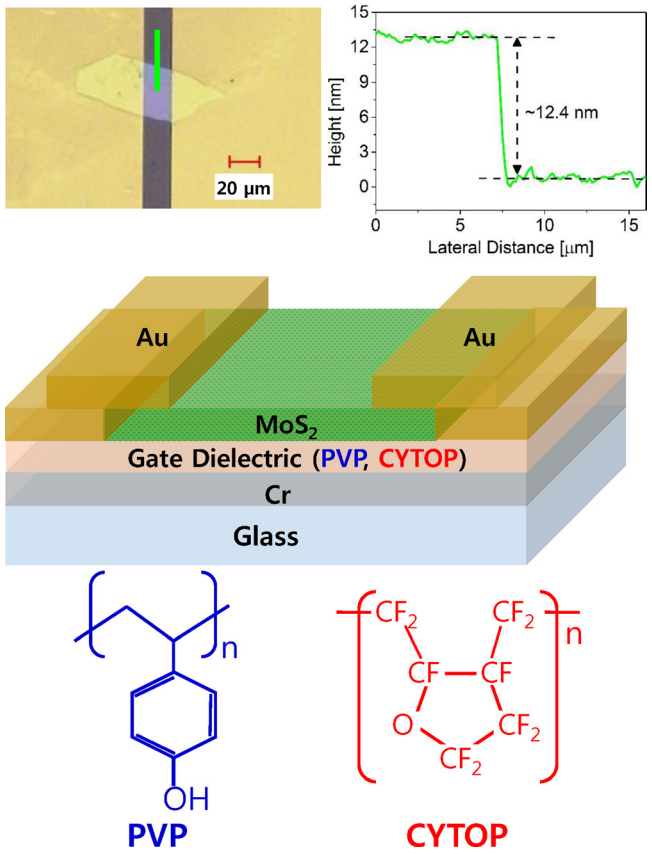

FIG. 1. 3D cross-sectional schematic view of MoS_2 FET with the polymer gate dielectric and its optical image with the AFM thickness profile (left). Chemical structures of the PVP (blue) and CYTOP (red) thin-films (right).

channel in Fig. 1 confirms the thickness of ~12.4 nm. Au (80 nm) as source/drain (S/D) electrodes was deposited by thermal evaporation and then patterned using conventional photolithography followed by wet chemical etching (Transene, GE-8148). The thickness of the MoS_2 channel and other device dimensions (W/L) were identified using AFM and an optical microscope, respectively. Current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed using a semiconductor parameter analyzer (HP 4156A) and Precision LCR meter (Agilent 4284A), respectively.

The characteristics of the prepared polymer layers as a gate dielectric are summarized in Table I. The thicknesses of the PVP and CYTOP dielectric layers were ~400 nm and ~280 nm, respectively, which were measured using the surface profiler (Tencor, P10). Both PVP and CYTOP layers exhibited quite smooth surface with rms roughness (Rq) of 5.0 and 6.8 Å measured by AFM, respectively. Capacitances (C) of 7.95 and 6.59 nF/cm^2 were obtained from C-V measurements for the MIM (Cr/polymer layer/Al stack) structure with a capacitor area of 2.76×10^{-3} cm^2 at 1 MHz as shown in Fig. 2(a), and the dielectric constants (ε_r) of 3.59 and 2.04 for PVP and CYTOP, respectively, were calculated from $\varepsilon_r = (C\ t)/(A\ \varepsilon_0)$, where C is the measured capacitance, A is the capacitor's area, t is the polymer dielectric thickness, and ε_0 is the vacuum permittivity. Finally, the surface energies of CYTOP and PVP were determined from contact angle measurements by Owens-Wendt Method using DI water and diiodomethane as probe liquids as summarized in Fig. 2(b).

TABLE I. Properties of the PVP and CYTOP films as a gate dielectric.

Gate dielectric	Film thickness	Capacitance (nF/cm^2)	ε_r	Surface roughness (R_q, Å)	Surface energy (mJ/m^2)
CYTOP	~280	6.59	2.04	6.8	21.5
PVP	~400	7.95	3.59	5.0	52.8

Figure 3(a) shows representative transfer curves of I_{DS}–V_{GS} for $V_{DS} = 1$ V, in which the effect of the CYTOP gate dielectric compared with PVP on the V_{TH} is clearly shown. The field-effect mobility (μ_{FE}) in a linear operation regime was extracted from $\mu_{FE} = L\ g_m/(W \cdot C_{OX} \cdot V_{DS})$, where W *is* a channel width, L is a channel length, C_{OX} is a capacitance of polymer dielectrics, and V_{DS} is drain bias of 1 V. Threshold voltage (V_{TH}) was calculated using a linear extrapolation method in a linear regime ($V_{DS} = 1$ V); it was found from the intercept of a tangent at the maximum g_m with V_{GS} axis. The MoS_2 FETs with the PVP dielectric show depletion-mode operation with significant negative V_{TH} of −14 V. On the contrary, the MoS_2 FETs with CYTOP exhibit an enhancement-mode with V_{TH} of 4.6 V, which means that the devices can be turned off at a zero gate bias. As a result, static power dissipation due to a leakage current and V_{TH} instability induced by negative gate-bias stress during the off-state can be minimized. Figure 3(b) represents output characteristics (I_{DS}-V_{DS}) for $V_{GS} = 0$, 5, 10, 15 V, exhibiting an ohmic-like linear behavior at low V_{DS} and saturation at high V_{DS} bias conditions.

The V_{TH} shift is attributed to the strong electron-withdrawing group (i.e., fluorine) in the chemical structure of CYTOP.[24,25] The molecular dipole field introduced by the fluorines in the end group can induce negative charges at the MoS_2-CYTOP interface, resulting in the shift of surface potential toward higher energy. UV photoelectron spectrometer measurement (AXIS Ultra DLD; Source: He I, 21.2 eV) was employed to convince and estimate a relative surface potential shift. To avoid charging effect, thin layer of both

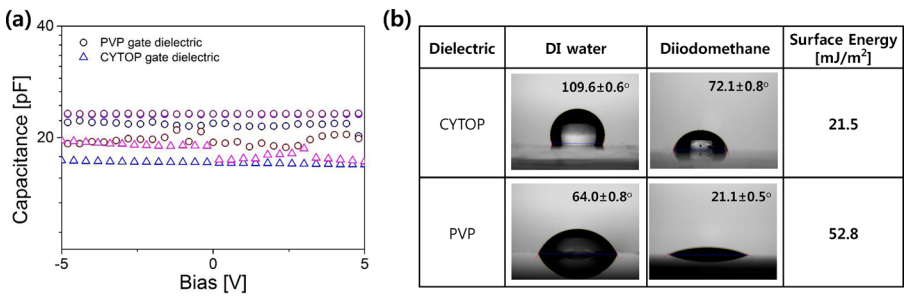

FIG. 2. (a) C-V measurements for MIM (Cr/polymer layer/Al stack) structure with a capacitor area of 2.76×10^{-3} cm^2 at 1 MHz using the LCR meter (Agilent 4284A). (b) Contact angle measurement of both gate dielectric surfaces, and calculated surface energies using the "Owens-Wendt Method."

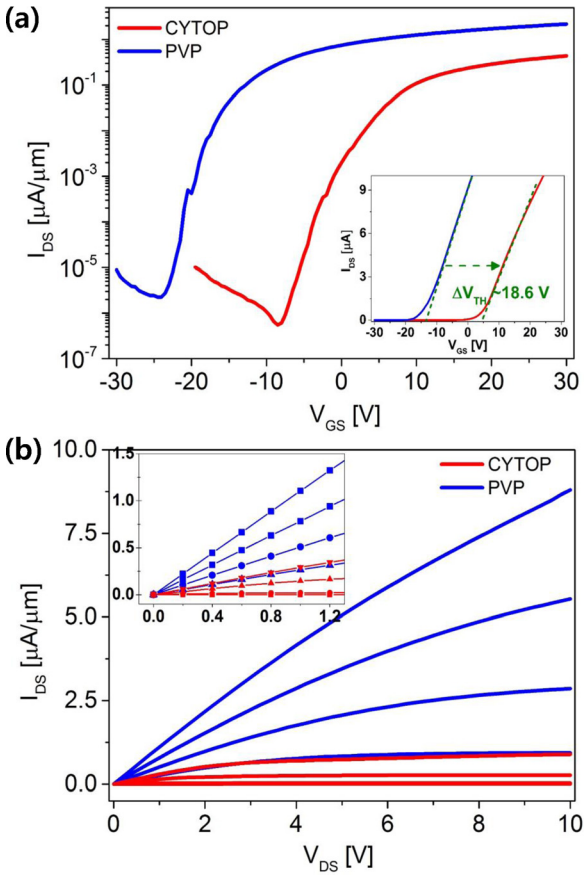

FIG. 3. (a) Transfer characteristics of the fabricated MoS_2 FETs with CYTOP (red) and PVP (blue) gate dielectrics for $V_{DS} = 1$ V. I_{DS} is normalized by the devices' channel width (W). (Inset) The transfer characteristics in a linear scale, in which positive V_{TH} shift is clearly shown. (b) Output characteristics (I_{DS}-V_{DS}) for $V_{GS} = 0$, 5, 10, 15 V, exhibiting good linearity at low V_{DS} (as shown in the inset) and saturation at high V_{DS} conditions.

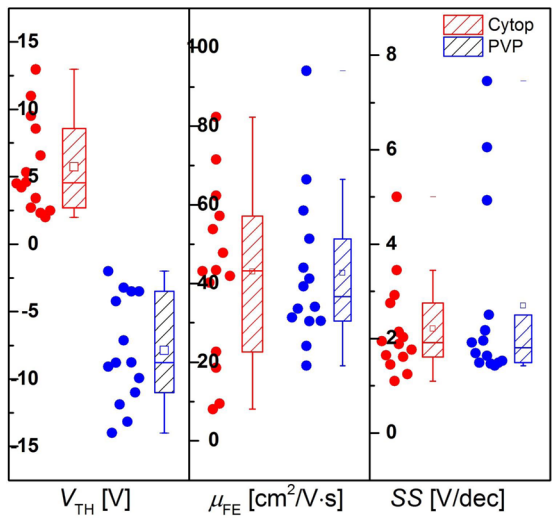

FIG. 5. Statistics of the electrical characteristics obtained from 14 devices. Threshold voltages (V_{TH}) of the measured MoS_2 FETs with CYTOP (red) and with of PVP (blue) dielectrics are distributed within 5.7 ± 3.5 V (enhancement mode) and -7.8 ± 4.0 V (depletion mode), respectively. However, there was no significant difference for field-effect mobility (μ_{FE}) and sub-threshold swing (SS).

polymer dielectrics (~13 nm) was prepared. Figure 4(a) shows that the onset point of secondary electrons from the CYTOP (4.50 ± 0.03 eV) was higher than the PVP (4.08 ± 0.08 eV). Therefore, the work function of the CYTOP is relatively higher than that of the PVP by 0.42 eV; mobile carriers in the channel were reduced or even depleted at zero gate-bias as explained using energy band diagram in Figs. 4(b) and 4(c). However, in the PVP or a typical oxide gate insulator, hydroxyl groups (-OH) and absorbed water molecules can induce surface charges at the gate dielectric, tuning the channel into accumulation regime.[26,27]

Furthermore, considering the performance variance induced by the MoS_2 thickness as well as fabrication process, multiple MoS_2 FETs were characterized in order to statistically compare electrical properties. Figure 5 shows the distribution of μ_{FE}, V_{TH}, and SS, which are also summarized in Table II. Above all, a depletion-mode with V_{TH} of -7.8 ± 4.0 V was exhibited for the PVP gate dielectric, and an enhancement-mode with V_{TH} of 5.7 ± 3.5 V for CYTOP. There was no significant difference of μ_{FE}, which might be attributed to the fact that even if PVP ($\varepsilon_r \sim 3.59$) has a higher dielectric constant than CYTOP's ($\varepsilon_r \sim 2.04$), other factors such as MoS_2 thickness, defects and other surface conditions affect μ_{FE} as well.[13,28] Distribution of SS, which were calculated from $SS = [d(\log_{10} I_{DS})/dV_{GS}]^{-1}$, indicates that the

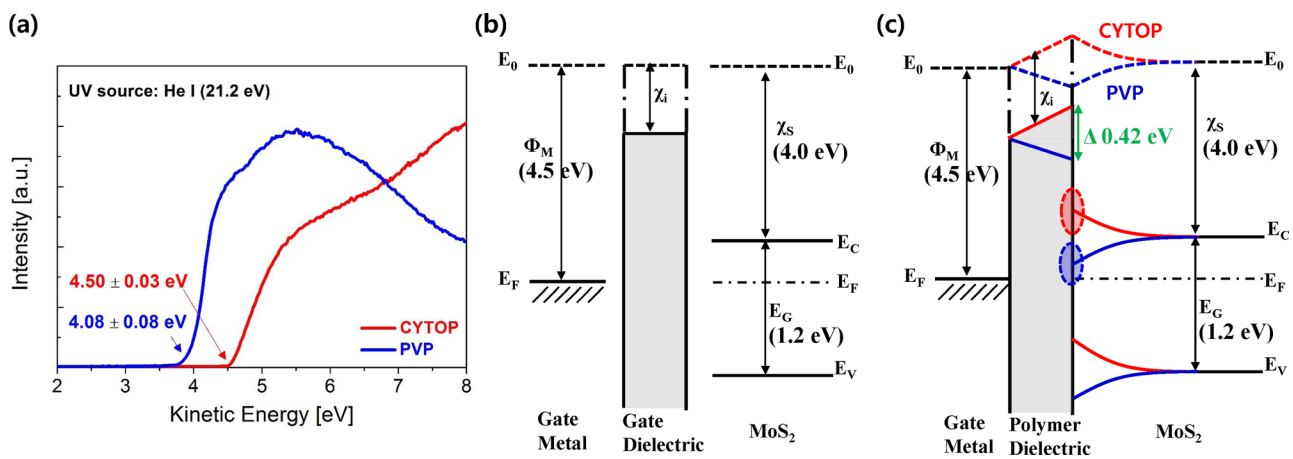

FIG. 4. (a) UPS spectrum of the CYTOP (red) and PVP (blue) gate dielectrics; a relatively higher onset point (0.42 eV) of CYTOP was observed in comparison to PVP. Schematic energy band diagram (b) of the typical isolated gate metal, gate dielectric, and MoS_2, and (c) of the fabricated MoS_2 FETs with the CYTOP (red) and PVP (blue) gate dielectrics with no applied gate voltage. MoS_2-PVP induces mobile carriers accumulated in the channel (i.e., depletion-mode), and MoS_2-CYTOP reduces and depletes mobile carriers in the channel (i.e., enhancement-mode).

TABLE II. Electrical parameters of the fabricated MoS_2 FETs (14 devices) containing PVP and CYTOP gate dielectrics, respectively.

Gate dielectric	V_{TH} (V)	μ_{FE} (cm^2/V s)	*SS* (V/dec)
CYTOP	5.7 ± 3.5	43.0 ± 22.3	2.2 ± 1.0
PVP	-7.8 ± 4.0	42.7 ± 19.7	2.7 ± 1.9

interface quality of MoS_2-PVP was similar to MoS_2-CYTOP interface.

In this work, we have fabricated and characterized enhancement-mode multilayer MoS_2 FETs using the amorphous fluoropolymer CYTOP as a gate dielectric. The fabricated devices exhibited positive V_{TH} of 5.7 ± 3.5 V with μ_{FE} of up to 82.3 cm^2/V s. In comparison, MoS_2 FETs with the cross-linked PVP dielectric showed a depletion-mode with V_{TH} of -7.8 ± 4.0 V. The surface dipole effect induced by the strong electron-withdrawing fluorine groups in CYTOP increases the surface potential by 0.42 eV, resulting in reduced mobile carriers in the channel and thus the positive shift of V_{TH}. The results suggest that the operation modes of multilayer MoS_2 FETs can be controlled by engineering the gate dielectric material. Furthermore, a direct-coupled FET logic based on MoS_2, which is a basic building block for low-power digital circuits, can be realized by integrating both enhancement- and depletion-mode MoS_2 FETs.

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