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Recent progress in high-mobility thin-film transistors based on multilayer 2D materials

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Abstract

Two-dimensional (2D) layered semiconductors are emerging as promising candidates for next-generation thin-film electronics because of their high mobility, relatively large bandgap, low-power switching, and the availability of large-area growth methods. Thin-film transistors (TFTs) based on multilayer transition metal dichalcogenides or black phosphorus offer unique opportunities for next-generation electronic and optoelectronic devices. Here, we review recent progress in high-mobility transistors based on multilayer 2D semiconductors. We describe the theoretical background on characterizing methods of TFT performance and material properties, followed by their applications in flexible, transparent, and optoelectronic devices. Finally, we highlight some of the methods used in metal-semiconductor contacts, hybrid structures, heterostructures, and chemical doping to improve device performance.

Keywords: 2D semiconductors, transition metal dichalcogenides, thin-film transistor, mobility, flexible, transparent, opto-electronics

(Some figures may appear in colour only in the online journal)

1. Introduction

The discovery of graphene opened the door to the intriguing electronic, optical, and mechanical properties of two-dimensional (2D) nanomaterials [1]. However, the semi-metallic nature of graphene makes it unsuitable for the application of conventional transistors for electronic switching. While a number of techniques have been suggested to open an energy band gap (E_g) in graphene, they are still far from being suitable for real applications [2]. As an alternative to graphene, a rapidly growing interest has been given to transition metal dichalcogenides (TMDs) with the formula of MX_2 (M = Mo, W; X = S, Se, Te) [3]. These materials form layered structures, where layers of covalently bonded X–M–X atoms are held together by van der Waals interactions. Due to the broken symmetry in the atomic basis, they become semiconductors with E_g of ~1 eV. Among these TMDs, molybdenum disulfide (MoS_2) has been most extensively investigated for transistor applications partly because of the availability of naturally-occurring crystals (molybdenite). While bulk MoS_2 is usually an *n*-type semiconductor with an indirect E_g (~1.3 eV) [4], monolayer MoS_2 has a direct E_g of ~1.8 eV [5, 6]. Field-effect transistors (FETs) based on monolayer or multilayer MoS_2 exhibit outstanding performance metrics, including high on/off-current ratio ($I_{on}/I_{off} \sim 10^7$), high mobility ($\mu \sim 100\,cm^2\,V^{-1}\,s^{-1}$), and low subthreshold swing ($SS \sim 70$ mV decade^{-1}) [7, 8].

However, the fabrication demands and the physics of MoS_2 suggest that multilayer MoS_2 can be more attractive for thin-film transistor (TFT) application than monolayer MoS_2. The synthesis of monolayer MoS_2 followed by the deposition of an additional high-*k* dielectric layer may not be well-suited

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for commercial fabrication processes. The density-of-states (DOS) of multilayer MoS_2 with a thickness of ~30 nm is three times that of monolayer MoS_2 [8], which will lead to considerably high driving currents in the ballistic limit. In long-channel TFTs, multiple conducting channels can be created by the field effect in multilayer MoS_2 for boosting the current drive of TFTs. Nonetheless, as most emphasis has been put on monolayer MoS_2 with little attention given to multilayer MoS_2, very few review articles on multilayer MoS_2 can be found in literature [9]. Here, we aim to review recent literature on high-mobility transistors based on multilayer TMDs and other 2D materials. We begin with summaries on the characterizations and the material properties of layered materials followed by their applications in flexible, transparent, and optoelectronic devices. Finally, we describe some of the important approaches used in metal-semiconductor contacts, hybrid structures, heterostructures, and chemical doping to enhance carrier mobility in 2D material transistors.

2. Theoretical background

High-mobility TFTs are essential for modern electronic devices, for example, active-matrix organic light-emitting diode panels for displays owing to their current-driving circuitry. In this regard, we begin this section with the most important characterizing methods of field-effect mobility (μ_{eff}) and intrinsic mobility (μ_0), which describe device characteristics and material properties, respectively, among various parameters. Then, we will review some common 2D materials for electronic device applications, and discuss the uniqueness in 2D material devices in comparison with conventional 3D-material-based transistors.

2.1. Characterization of TFT performance: μ_{eff} versus μ_0

Although the transport physics in TFTs is different from that in metal oxide semiconductor field effect transistors (MOSFETs) [10, 11], the relation among the drain–source current (I_{ds}), gate–source voltage (V_{gs}), and drain–source voltage (V_{ds}) can be described using a conventional formula as:

$$I_{\text{ds}} = \frac{\mu_{\text{eff}} W C_{\text{GI}}}{L}\left[(V_{\text{gs}} - V_{\text{th}})V_{\text{ds}} - \frac{V_{\text{ds}}^2}{2}\right] \tag{1}$$

where W and L are the channel width and length, C_{GI} is the capacitance per unit area of gate insulator (GI), and V_{th} is the threshold voltage, respectively [10–12]. Equation (1) is valid only for the linear regime ($|V_{\text{ds}}| < |V_{\text{gs}} - V_{\text{th}}|$). Other parametric information and details for the saturation regime ($|V_{\text{ds}}| > |V_{\text{gs}} - V_{\text{th}}|$) are reported elsewhere [10–13]. Considering the standard model of MOSFETs and the parallel plate model of gate capacitance, the μ_{eff} of the TFT can be calculated as below [14].

$$\mu_{\text{eff}} = \frac{L}{W C_{\text{GI}} V_{\text{ds}}}\frac{\mathrm{d}I_{\text{ds}}}{\mathrm{d}V_{\text{gs}}}\bigg|_{V_{\text{ds}}}. \tag{2}$$

Most widely adopted TFT architectures exhibit two-terminal configuration of source/drain (S/D) electrodes [10, 11, 13]. Therefore, μ_{eff} and I_{ds} are generally underestimated compared to the intrinsic capability of the materials due to the contact resistance between the active layer and S/D electrodes. Ghibaudo proposed the *Y*-function method, enabling an extraction of μ_0 excluding any contact resistance terms [15], in which equation (1) can be modified as below:

$$I_{\text{ds}} = \frac{W C_{\text{GI}}}{L}\frac{\mu_0}{[(1 + \eta(V_{\text{gs}} - V_{\text{th}})]}(V_{\text{gs}} - V_{\text{th}})V_{\text{ds}} \tag{3}$$

where η is the mobility reduction coefficient. Because the transconductance is defined as a differentiation of I_{ds} with respect to V_{gs} $\left(g_m \equiv \frac{\partial I_{\text{ds}}}{\partial V_{\text{gs}}}\Big|_{V_{\text{ds}}}\right)$, we can express it as below:

$$g_m = \frac{W}{L} C_{\text{GI}} \frac{\mu_0}{[1 + \eta(V_{\text{gs}} - V_{\text{th}})]^2} V_{\text{ds}}. \tag{4}$$

The basic concept of the *Y*-function method is mathematically eliminating the η by combining equations (3) and (4).

$$Y = \frac{I_{\text{ds}}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} C_{\text{GI}} \mu_0 V_{\text{ds}}}\,(V_{\text{gs}} - V_{\text{th}}). \tag{5}$$

Finally, μ_0 can be obtained from the slope of the Y–V_{gs} curve as below:

$$\mu_0 = \frac{L}{W}\frac{[\text{Slope}]^2}{C_{\text{GI}} V_{\text{ds}}}. \tag{6}$$

2.2. Common 2D materials for electronic device applications

A transistor is the fundamental building block of today's semiconductor electronics. Figure 1(a) presents μ_{eff} of the various 2D material TFTs in recent reports as a function of the corresponding E_{g} [7, 8, 16–32]. Graphene is well known for its ultra-high carrier mobility [1, 33, 34], and this excellent electrical property results from the linear dispersion relationship or zero effective mass [35]. However, due to the absence of E_{g}, electronic devices based on graphene cannot be completely turned off, limiting the $I_{\text{on}}/I_{\text{off}}$ to be around one order of magnitude [2, 36]. In order to overcome this limitation, various methods have been proposed to open a bandgap in graphene: tailoring graphene into nanoribbons [21, 22, 37] or applying a large vertical electric field to bilayer graphene [18, 20, 38]. However, all these methods are accompanied by a drastic reduction in mobility [2, 20–22]. Nevertheless, the high carrier mobility of graphene makes it promising for radio-frequency (RF) analogue device applications (figure 1(b)) [39–41]. Graphene-based RF circuit blocks such as frequency multipliers [42] and multi-modulation wireless circuits [43] have been demonstrated, where graphene transistors have fulfilled the requirements and expectations by exhibiting intrinsic cut-off frequency (f_{T}) comparable to the best values of III–V transistors and by surpassing silicon (Si)-based transistors at comparable gate lengths [44–46]. A high f_{T} of 427 GHz

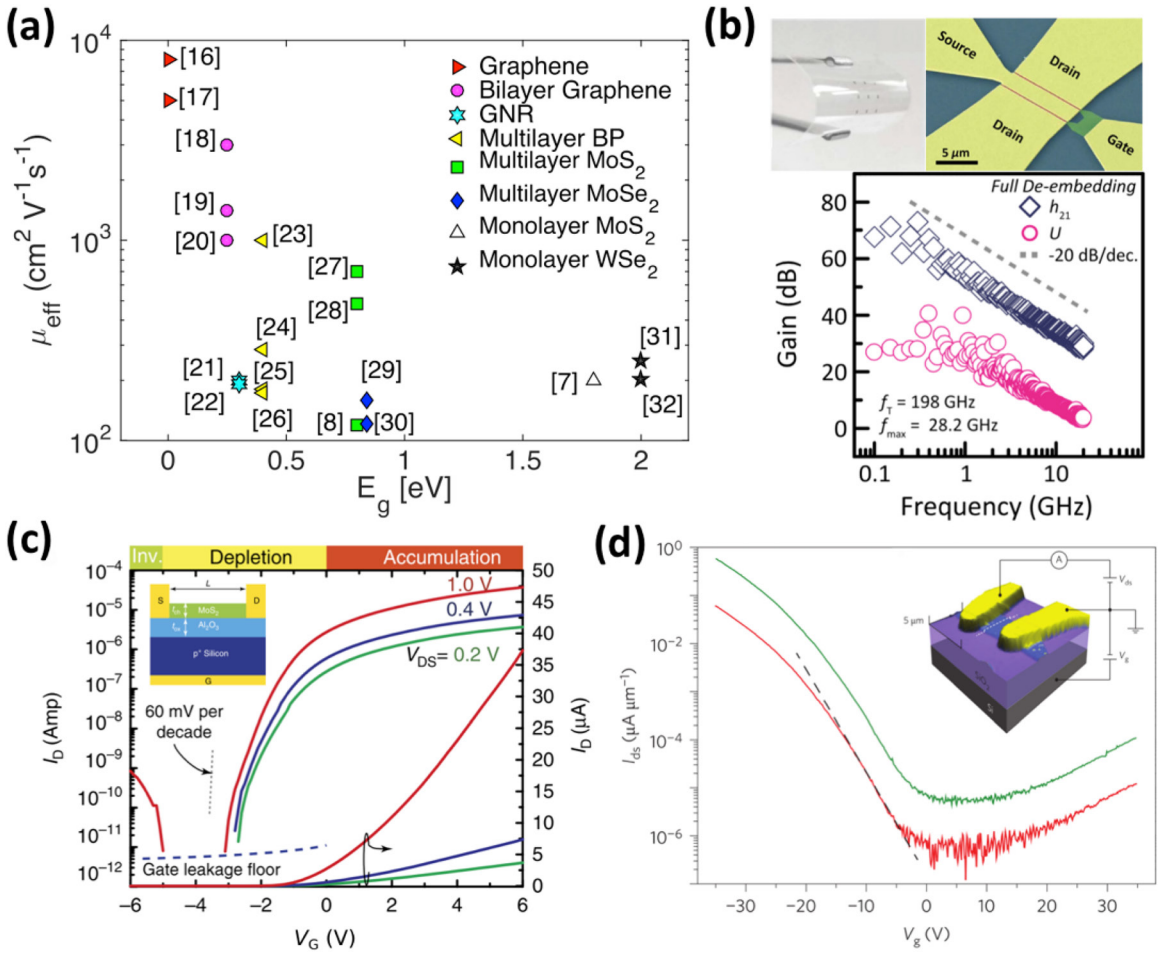

Figure 1. (a) μ_{eff} versus E_g for various 2D material TFTs (mostly *n*-type transistors except for BP TFTs) at RT; graphene [16, 17], bilayer graphene with a vertical electric field [18–20], graphene nanoribbon with a width of <10 nm [21, 22], multilayer BP [23–26], multilayer MoS_2 [8, 27, 28], multilayer $MoSe_2$ [29, 30], monolayer MoS_2 [7], monolayer WSe_2 [31, 32]. (b) RF characteristics of a flexible graphene TFT after de-embedding. Reproduced with permission from [39]. Copyright 2014 IEEE. (c) Transfer characteristics of a multilayer MoS_2 TFT, showing I_{on}/I_{off} of ~10^6 and *SS* of ~80 mV dec^{-1}. Reprinted by permission from Macmillan Publishers Ltd: Nature Communications [8], Copyright 2012. (d) Ambipolar multilayer BP TFT. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [23], Copyright 2014.

has been achieved on a 67 nm-gate graphene transistor [47], but the maximum oscillation frequency (f_{max}) is still significantly limited to below 50 GHz due to parasitic effects [45, 46, 63].

On the other hand, for switching device applications, both moderate E_g and high mobility are critical. In this regard, among many layered materials shown in figure 1(a), TMDs (figure 1(c)) and black phosphorus (BP) (figure 1(d)) stand out. The μ_{eff} of TMDs is relatively lower (~100 cm^2 V^{-1} s^{-1}) [8, 31, 48] than that of BP, but its high I_{on}/I_{off} (10^8–10^{10}) [31, 32, 49] is appealing for ultra-low-power transistors. In comparison, BP has a higher μ_{eff} in the range of a few hundreds to over 1000 cm^2 V^{-1} s^{-1}, but a relatively lower I_{on}/I_{off} (10^5–10^8) has been reported so far with multilayer BP transistors [23–25], making it more attractive for high performance logic transistors [50].

Compared to conventional 3D semiconductors, one of the key advantages of 2D materials is that it provides a fully terminated surface without dangling bonds. This can allow the fabrication of devices avoiding detrimental surface states and charge traps, from which III–V semiconductors are currently suffering [51]. Because of the absence of dangling bonds, very low *SS* (~70 mV dec^{-1}) can be achieved with 2D material transistors, which is comparable to those of the state-of-the-art Si transistors [8, 52]. The excellent switching characteristics in 2D materials are also directly related to their inherent thinness since it guarantees the excellent electrostatic control by the gate electrode on the entire channel region in a transistor. Unlike the conventional 3D materials, where artificially made thin geometries (such as silicon-on-insulator or FinFET structure) [53–55] will be needed to avoid significant leakage current, layered materials inherently provide large immunities to short-channel effects [56].

Another unique feature in 2D material TFTs is that the number of layers has a significant impact on device performance, in contrast to conventional 3D material transistors, as it can affect the overall properties of band structure including E_g, effective mass, and DOS. In general, higher number of layers means larger DOS and multiple conducting channels, which can lead to a higher on-state current [8, 57]. In addition, since the bandgap changes with the number of layers (monolayer

2D material usually has a larger E_g than its bulk form), there is flexibility to engineer the number of layers for particular target applications: for example, BP has a tunable E_g from 0.3 eV in bulk to ~2.0 eV in monolayer, offering various device applications from high-performance to low-power transistors [58–60]. As the number of layers changes, the nature of the bandgap changes from direct to indirect or vice versa for TMDs [61–63], whereas BP always provides a direct band gap regardless of its thickness [58, 59, 64]. The variation of effective mass with the number of layers is another factor to consider when designing FETs based on layered materials [58, 61, 65].

2D materials can also be promising for flexible electronics with plastic substrates due to their excellent mechanical flexibility and the compatibility with low-temperature fabrication processes [63, 66, 67]. Using 2D materials for flexible electronics can overcome several technical challenges in other material systems, including low mobility (typically below 10 cm^2 V^{-1} s^{-1}), high drive voltage of organic materials [68, 69], complex technological processes, and large leakage current with polycrystalline Si [63, 70, 71]. A flexible graphene transistor with $f_T = 198$ GHz and $f_{max} = 28$ GHz was demonstrated for flexible RF and analogy applications [39]. A flexible BP transistor with a superior μ_{eff} of ~300 cm^2 V^{-1} s^{-1} and I_{on}/I_{off} of ~10^4 was also developed for an amplitude-modulated (AM) demodulator [72].

3. Applications of 2D TMDs TFTs

In this section, we introduce recent research reports on various applications of multilayer TMD TFTs, especially focusing on flexible, transparent, and photo-sensing/detecting devices beyond the capacity of conventional devices. Flexible and transparent devices by themselves occupy significant positions in the fundamental sciences and industrial applications. Moreover, it is highly expected that great synergies can be made by integrating with other devices for various applications including energy harvesting, sensing, and optoelectronic devices.

3.1. Flexible devices

Flexible electronics should endure harsh environments, including various mechanical stresses (bending, folding, rolling, and stretching), a wide range of temperature/humidity, and other operating conditions while maintaining their normal device performances [73, 74]. It should be noted that some 2D materials are known to be easily oxidized and weak to humidity. For example, the surface of the BP is hydrophilic and oxidizable, which can lead to degradation of the device performance [75–77]. However, atomic-layer-deposited (ALD) aluminum oxide (Al_2O_3) or hexagonal boron nitride (*h*BN) can be integrated for surface passivation with good mechanical properties [72, 78], which increases thermal stability (−263 to 150 °C) [79, 80] and extends device lifetime to a couple of months under ambient conditions [79–82]. In order to satisfy the requirements for flexible electronics, the individual components constituting flexible TFTs (e.g. substrate, gate electrodes, semiconductors for the active layer, GI, and S/D electrodes) must be both mechanically and electrically stable with respect to external stimuli.

The most commonly used flexible substrates are poly (methyl methacrylate), polyether sulfone, polyethylene naphthalate (PEN), polyethylene terephthalate (PET), and polyimide (PI), etc [83]. However, PEN or PET are easily deformed at around 100–150 °C, which would be a critical obstacle for fabricating flexible devices through the conventional Si TFT processes (up to ~500 °C). In addition, TFTs incorporating TMDs necessitate post-thermal annealing under inert gas environments (>250 °C) to improve their device performance through the reduction of the contact resistance [8, 14]. Thus, PI would be appropriate for the fabrication of high performance flexible devices considering its outstanding decomposition temperature (~600 °C) as well as good chemical and mechanical stability [83–85].

For active materials in flexible TFTs, multilayer TMDs including MoS_2 and molybdenum diselenide ($MoSe_2$) can be suggested as fascinating alternatives of hydrogenated amorphous Si (a-Si:H) or low temperature poly-Si, owing to their excellent mechanical properties (Young's modulus 240–270 GPa), decent μ_{eff} (>100 cm^2 V^{-1} s^{-1}), and wide spectral responses [3, 7, 8, 14, 74, 86, 87]. On the other hand, alternatives for flexible electrodes have to satisfy the follwing requirements: (1) electrical properties should be maintained under various mechanical stresses. (2) Surface roughness of the entire electrode area must be sufficiently small in order to guarantee fast carrier transport along the active layers grown above them. (3) Flexible electrodes must be attached well on the individual components of the TFTs resulting in confident contacts at adjacent intersections. Potential candidates include poly (3,4-ethylenedioxythiophene):poly (4-styrenesulfonate) [88–90], metal grids [91], graphene [92–94], carbon nanotubes [95, 96], nanotube/polymer composites [97–99], and a 2D random network of metal nanowire (NW) [100–104]. After the fabrication of flexible TFTs, appropriate detaching procedures, for example, dissolution of the sacrificial layer [105] or excimer laser treatment [106, 107], may be necessary when the flexible substrates are formed on rigid carrier substrates to use conventional TFT processes. In addition, the concept of the neutral mechanical plane can be applied in order to optimize mechanical flexibility by adjusting a stress-free zone to a stress-vulnerable position within the flexible TFT [108–112].

Table 1 presents a list of typical features of the various flexible MoS_2 TFTs in literature. The μ_{eff} values of the flexible TFTs are less than 10 cm^2 V^{-1} s^{-1} [113, 114], and μ_0 extracted by the *Y*-function method are higher than 15 cm^2 V^{-1} s^{-1} [105, 115–117]. Tri-layer MoS_2 TFTs fabricated by using *h*BN as a GI and graphene as a gate electrode, exhibit μ_{eff} of ~45 cm^2 V^{-1} s^{-1} for the rigid Si substrate and 29 cm^2 V^{-1} s^{-1} for the flexible PEN substrate, respectively, without post-thermal annealing [118].

Kim and coworkers reported on the flexible multilayer MoS_2 TFTs using a PEN substrate, as shown in figure 2(a) [119]. Indium thin oxide (ITO, 100 nm) and a stack of ALD Al_2O_3 (50 nm) followed by sputter-deposited silicon dioxide (SiO_2, 250 nm) were used as the bottom-gate electrode and GI,

Table 1. Typical features of various flexible MoS_2 TFTs.

Active MoS_2 (# of layer)	Flexible substrate	GI	Electrodes	μ_{eff} / μ_0 [a] ($cm^2\ V^{-1}\ s^{-1}$)	I_{on} / I_{off}	Ref.
CVD (1L)	HfO_2 passivated PI	Al_2O_3	S/D: Graphene, G: Au	18.9 ± 1.1[a]	10^7	[115]
CVD (1L)	HfO_2 passivated PI on Kapton film	HfO_2	S/D: Ag/Au, G: Pd	22[a]	10^5	[116]
CVD (3L)	PI	Ion gel	S/D: Ni/Au, G: Ni/Au	3	10^3	[113]
Exfoliated (3L)	PEN	*h*-BN	S/D: Ti/Au, G: Graphene	29	10^5	[118]
Exfoliated (3.5 nm)	PI	Al_2O_3	S/D: Au, G: Cu	19[a]	10^6	[105]
Exfoliated (10 nm)	PI on Kapton film	Al_2O_3 or HfO_2	S/D: Ti/Au, G: Ti/Pd	30[a]	10^7	[117]
Exfoliated (58 nm)	PET	*c*-PVP	S/D: Graphene, G: ITO	4.7 ± 3.3	$\sim 5 \times 10^4$	[114]
Exfoliated (30–80 nm)	PEN	Al_2O_3/SiO_2	S/D: Ti/Au, G: Ti/Al	$\sim 35 \pm 10$	10^7	[30]
Exfoliated (79.3 nm)	PI	SU-8/Al_2O_3	S/D: Ti/Au, G: Ag NWs[b]	141.3	5×10^5	[104]

[a] Low-field mobility (μ_0) extracted using the *Y*-function method.
[b] Laser-welded Ag NWs bilaterally embedded between the PI substrate and the SU-8 layer.

respectively. Then, mechanically exfoliated multilayer MoS_2 flakes with thicknesses of 30–80 nm were transferred onto the stacked GI, and S/D electrodes were patterned by using titanium (Ti, 10 nm) and gold (Au, 300 nm) through the photolithography and lift-off techniques. In order to overcome the low thermal budget of the PEN substrate, the authors utilized a picosecond pulse laser, which was selectively irradiated on the contact regions between the S/D electrodes and the active layer (bottom left corner of figure 2(a)) inducing localized thermal annealing effects without deteriorating the PEN substrate. Transfer (I_{ds}–V_{gs}) and output (I_{ds}–V_{ds}) characteristics shown in figure 2(a) clearly demonstrated the influences the selective laser annealing treatments had on contact regions of the flexible TFTs. The μ_{eff} of the devices was increased from $\sim 15 \pm 10\ cm^2\ V^{-1}\ s^{-1}$ (before) to $\sim 35 \pm 10\ cm^2\ V^{-1}\ s^{-1}$ (after laser annealing). These results were attributed to the solid-state diffusion of Ti into MoS_2 and the formation of more conducting Ti-MoS_2 interlayers [120, 121], which reduced the Schottky barrier (SB) width and contact resistance.

As shown in figure 2(b), Rhyee *et al* reported on the flexible multilayer $MoSe_2$ TFTs using a PI substrate [30]. Ti (20 nm)/aluminum (Al, 50 nm) on a PI substrate was patterned to form bottom-gate electrodes, and then an organic SU-8 solution was spin-coated with thicknesses of 600–650 nm for flexible GIs. Multilayer $MoSe_2$ flakes were mechanically exfoliated from a modified chemical vapor deposited (CVD) single crystalline platelet and transferred onto the organic GI. S/D electrodes were fabricated through the photolithography and etching of the Ti/Au (20 nm/100 nm) layer. The authors presented the μ_{eff} of $\sim 80\ cm^2\ V^{-1}\ s^{-1}$ for their flexible TFT, which was quite comparable to μ_0 of $89.1 \pm 4.29\ cm^2\ V^{-1}\ s^{-1}$ for other TFTs on the rigid Si substrate with SiO_2 GI. The flexible multilayer $MoSe_2$ TFTs also exhibited solid tolerance against tensile stresses due to the upward static bending parallel to the active channels as shown in the transfer characteristics under flat and bent conditions with a bending radius (r) of 10 and 5 mm.

Recently, Hong and coworkers demonstrated highly flexible multilayer MoS_2 TFTs on a PI substrate with outstanding device performances, which were accomplished with the aid of a 2D random network of silver (Ag) NWs and a hybrid organic/inorganic bilayer, as shown in figure 3 [104]. The authors utilized picosecond pulse laser treatment for enhancing electrical properties of the Ag NWs network through the plasmonic welding of the multi-junctions, which decreased the sheet resistances from $480 - 550\ \Omega\ sq^{-1}$ (before) to $10 - 15\ \Omega\ sq^{-1}$ (after laser welding). Clever control of the fabricating procedures shown in figure 3(a) enabled the Ag NWs network to embed bilaterally between the PI substrate and the organic SU-8 layer in the hybrid bilayer GI (e.g. PI/Ag NWs/SU-8), which guaranteed a damage-free detachment of the 2D Ag NWs network/PI composite from the rigid substrate without any sacrificial layer or excimer laser treatment. This bilaterally embedded sandwich structure also supported a tolerance against mechanical stresses and maintaining electrical properties of the NWs. In addition, the high-*k* ALD Al_2O_3 layer could compensate rather poor adhesion between the organic surface and the metal S/D electrodes. As shown in figure 3(c), transfer characteristics of the flexible TFTs under the initial flat condition showed that maximum μ_{eff} and I_{on}/I_{off} reached up to $141.3\ cm^2\ V^{-1}\ s^{-1}$ and $\sim 10^6$, respectively. Output characteristics of the same device revealed Ohmic contacts between the active layer and the S/D electrodes at a low V_{ds} regime with robust current saturation at a high V_{ds} regime. Such superior performances of the flexible TFT were attributed to the post-thermal annealing (>250 °C).

Variation of the device performances were studied through static and cyclic modes of upward bending, which were applied to the flexible TFT array parallel to their active channels. The lamination of the PET film with a thickness of 100 μm beneath the PI substrate resulted in the down-shift of the neutral plane, i.e. the entire TFT lay within the tensile-stress zone indicating that the flexibility was estimated under much harsher environments. Figure 3(d) compared the transfer characteristics of the flexible TFT array under flat and statically bent conditions with the r of 10 and 5 mm. The variation of the mobility values ($\Delta\mu\ (\%) = |\mu_{bending} - \mu_{flat}|/\mu_{flat}$) were estimated to be 2.0% ($r = 10$ mm) and 8.8% ($r = 5$ mm), respectively. V_{th} in the flat condition was estimated to be −18.7 V. For $r = 10$ mm, the V_{th} just remains identical to its initial value, and shifted to −19.5 V when $r = 5$ mm. Figure 3(e) presented a comparison of the transfer characteristics of another flexible TFT under cyclic bending. As the number of bending cycles (n) increases, the entire I_{ds}–V_{gs} curves shifted slightly toward the negative V_{gs} region, whereas the I_{on}/I_{off} was preserved

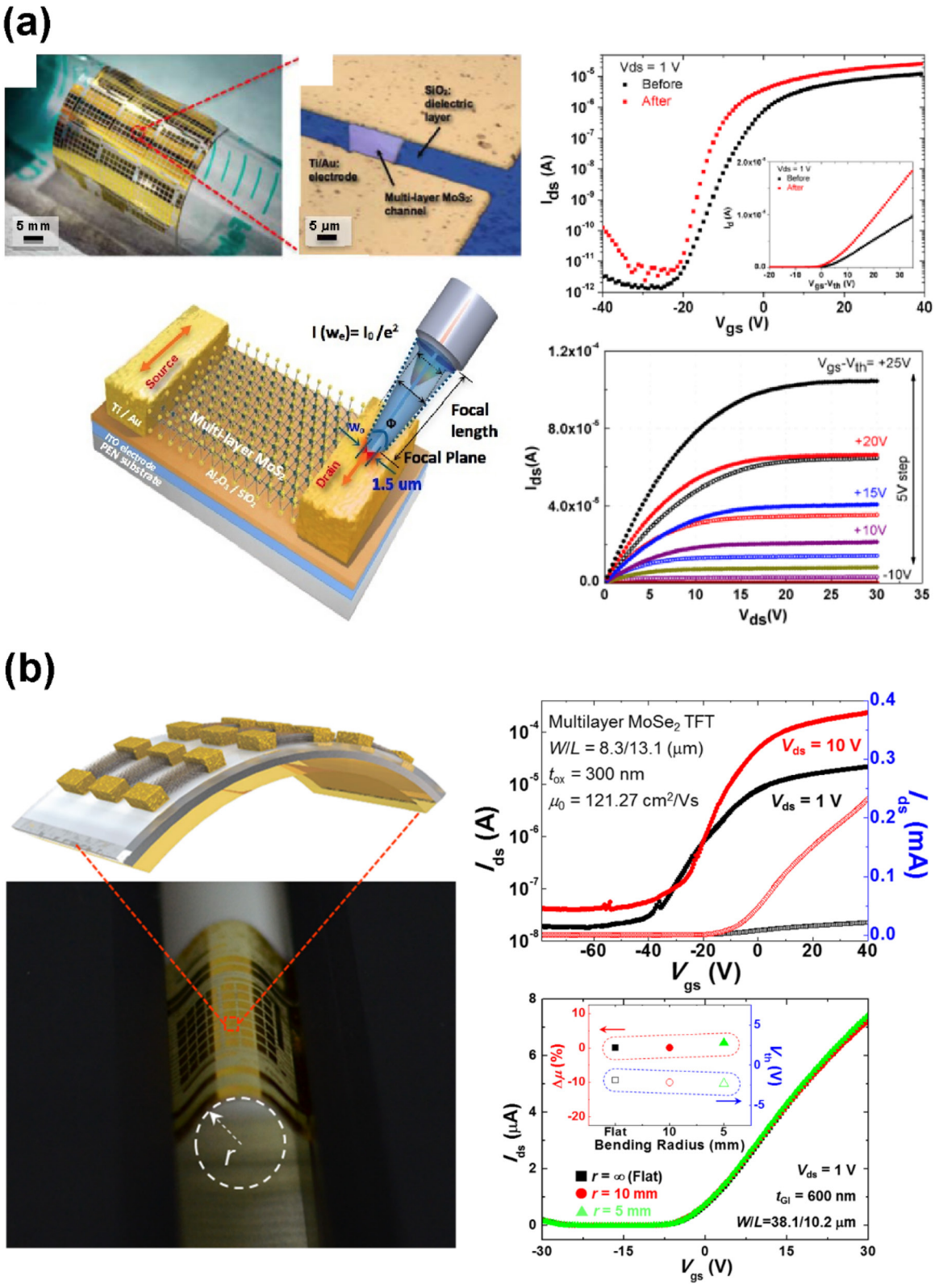

Figure 2. (a) Flexible multilayer MoS_2 TFTs using a PEN substrate. (Left bottom) Schematic illustration of the picosecond pulse laser annealing system for enhancing contacts between S/D electrodes and the active layer. (Left top) Photograph of the bent TFTs array with a bending radius of 15 mm. Inset: magnification of a unit TFT using a 3D laser confocal microscope. (Right top) Comparison of the transfer characteristics of the flexible TFTs depending on selective laser annealing treatments on contact regions. Inset: $I_{ds} - (V_{gs} - V_{th})$ curves in linear scale. (Right bottom) Output characteristics of the flexible TFTs before (open circles) and after (solid circles) laser annealing. Reproduced from [119], Copyright 2014 Tsinghua Univ. Press. With permission of Springer. (b) Flexible CVD grown multilayer $MoSe_2$ TFTs using a PI substrate. (Left) Photograph of the flexible TFTs array loaded in the multimodal bending system. White-dashed circle defines a designated bending radius. Inset: schematic cross-section of the flexible TFTs array in perspective view. (Right top) Transfer characteristics of the CVD grown $MoSe_2$ TFT on a rigid substrate. (Right bottom) Comparison of the I_{ds}–V_{gs} curves of the flexible TFT with respect to static bending radius. Inset: variations of $\Delta\mu$ and V_{th} for the flexible TFT under mechanical stress due to the different bending radii. Rhyee *et al* [30] John Wiley & Sons. Copyright 2016 Wiley-VCH Verlag GMBH.

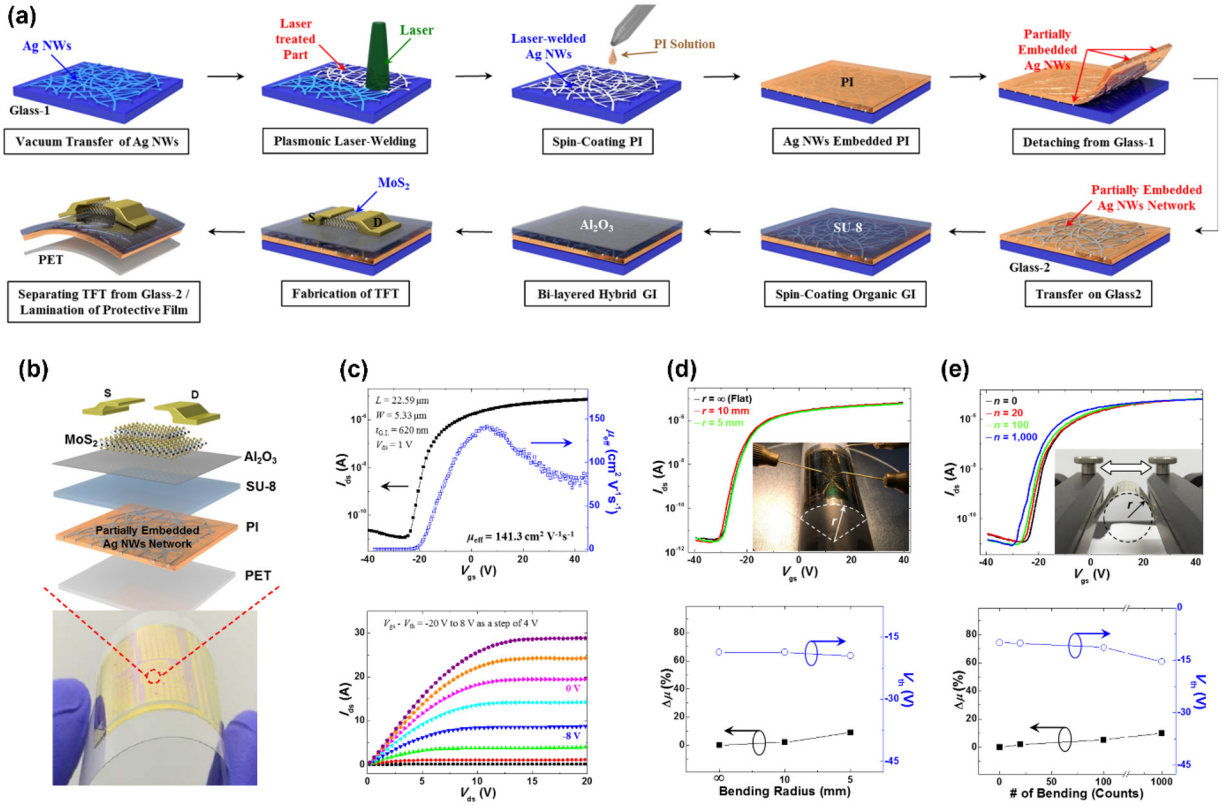

Figure 3. (a) Schematic flow chart of the flexible multilayer MoS_2 TFTs fabrication, which consists of the laser welded/embedded 2D Ag NWs network, solution-based thin PI, and an organic/inorganic hybrid GI. (b) Photograph of the bent flexible TFTs array. A transparent PET film was laminated beneath the PI substrate. Inset: schematic layer-by-layer structure of the flexible TFT. (c) Electrical properties under the initial flat condition. (Top) Transfer characteristics and μ_{eff} of the flexible TFT at $V_{ds} = 1$ V. (Bottom) Output characteristics of the same TFT under different V_{gs}. (d) and (e) Variation of the TFT performances under (d) static and (e) dynamic bending environments (tops) comparison of the transfer characteristics under (d) three different bending radii and (e) cyclic bending with respect to the number of bending cycles. Insets: photographs of the flexible TFTs loaded on (d) rigid cylinder with a predefined radius and (e) multimodal bending tester, respectively. (Bottoms) Variations of μ_{eff} and V_{th} as a function of the (d) static bending radii and (e) number of cyclic bending. Song *et al* [104] John Wiley & Sons. Copyright 2016 Wiley-VCH Verlag GMBH & Co. KGaA, Weinheim.

to ~10^5. The $\Delta\mu$ (V_{th}) due to the cyclic bending with n of 20, 100, and 1000 were estimated to be 1.9% (−10.1 V), 5.3% (−11.3 V), and 10.0% (−15.4 V), respectively. The authors claimed that the flexibility would be further improved by optimizing the position of the neutral plane into the stress-vulnerable layer, which could be conducted through lamination of an additional protective layer with the appropriate thickness on top of the current device stack.

3.2. Transparent devices

To realize a next-generation transparent display, fully transparent TFTs will be indispensable because the TFT backplane in the display panel plays a major role to diminish the optical transmittance [122]. Especially, electrodes in TMDs TFT have been one of the major performance limiting factors due to non-negligible Schottky barrier height (SBH) [8, 14, 27, 123]. It should be noted that alternatives of flexible electrodes, discussed in section 3.1, can also be utilized for those of the transparent electrodes. Recent studies reported that hetero-contacts/structures between TMDs and graphene electrodes can provide high performance transparent contacts due to their structural similarity without dangling bonds and unique 2D–2D interface, resulting in a small SBH [124, 125]. In spite of these significant progresses in the related research fields, critical weaknesses still exist, such as a trade-off between electrical properties and optical transparency, large-area growth, and processibility, which may limit their potential applicability to commercial integrated circuitry and devices. On the other hand, transparent conducting oxides (TCOs), such as ITO or indium zinc oxide (IZO), can be another contender, as they show excellent optical transmittance over a wide spectral range and compatibility to conventional TFT processes.

As another important factor for transparent display, active materials of the TFTs in the display backplane should stand light generated from illuminating components, e.g. a backlight unit in liquid crystal display. In this regard, multilayer TMDs, especially MoS_2, would be advantageous due to their indirect energy band nature [3, 8, 14, 87] resulting in much less vulnerable characteristics against incident light (see more details in section 3.3).

Kim and coworkers reported on transparent multilayer MoS_2 TFTs using TCOs as transparent electrodes, as shown in figure 4(a) [126]. ITO-glass was used for the bottom-gate electrode as well as a transparent substrate. Mechanically exfoliated multilayer MoS_2 flakes and IZO patterns were used for active layers and transparent S/D electrodes, respectively.

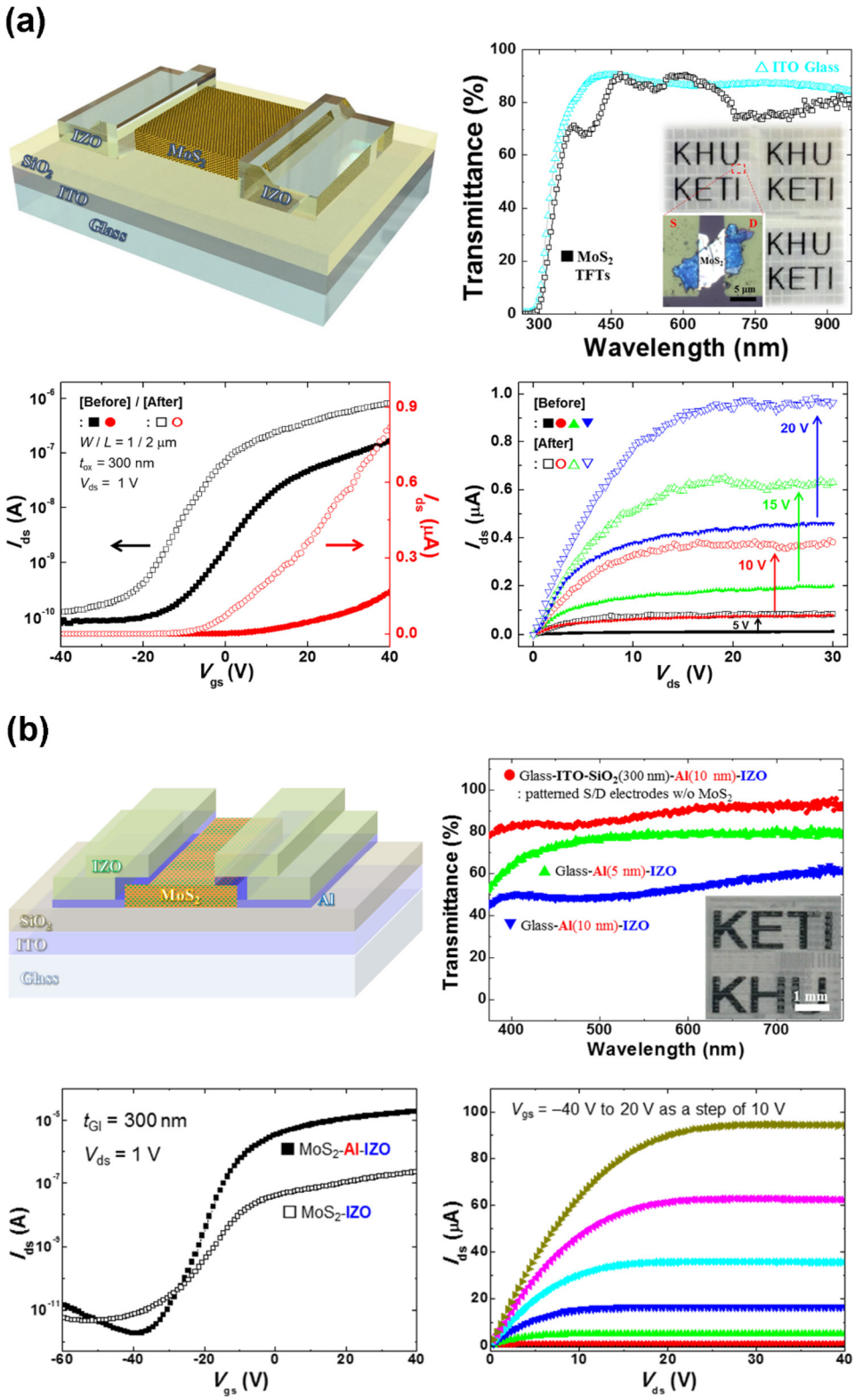

Figure 4. (a) Transparent multilayer MoS_2 TFTs through laser annealing treatment. (Left top) Schematic illustration of the device in perspective view. (Right top) Comparison of the transmission spectra of the ITO glass and the transparent TFTs. Inset: optical microscope images of the transparent TFTs array on the printed texts and magnification of the red-dashed box showing a single TFT consisting of a multilayer MoS_2 flake between the IZO S/D electrodes. (Left bottom) Transfer characteristic curves before (solid) and after (open symbols) laser annealing. (Right bottom) Output characteristic curves before (solid) and after (open symbols) laser annealing. Reproduced from [126]. (b) Transparent multilayer MoS_2 TFTs using low work function metal layer. (Left top) 3D schematic illustration of the device. (Right top) Comparison of the transmission spectra of the the TFT configuration using patterned Al-IZO including ITO-SiO_2 layers and continuous bi-layers of Al-IZO with different Al thicknesses. Inset: photograph of the TFT patterned Al-IZO bi-layer on the printed texts. (Left bottom) Transfer characteristic curves without and with the Al layer. (Right bottom) output characteristic curves of the transparent TFT with the Al intercalating layer. Reproduced from [130].

Table 2. Comparison of photoresponsivities (R) of various MoS_2 TFTs.

Active MoS_2 (# of Layer)	Bias	Illumination	R (A W^{-1})	Gate	Ref.
CVD film (1L)	$V_{ds} = 1$ V, $V_{gs} - V_{th} = 100$ V	$\lambda = 532$ nm, $P = 0.13$ mW cm^{-2}	780 / 2200[a]	Global bottom	[134]
Exfoliated flake (1L)	$V_{ds} = 8$ V, $V_{gs} = -70$ V	$\lambda = 561$ nm, $P = 24$ μW cm^{-2}	880	Global bottom	[135]
Exfoliated flake (1L)	$V_{gs} = 100$ V	$\lambda = 532$ nm, $P = 5$ nW	10^3	Global bottom	[137]
Exfoliated flake (2L)	$V_{ds} = 5$ V	$\lambda = 532$ nm, $P = 0.9$ nW	~10	Global bottom	[137]
CVD film (4L)	$V = 3$ V	$\lambda = 532$ nm, $P = 100$ mW cm^{-2}	0.12 / 0.55[b]	Two terminal	[138]
Film by thermolysis (few-layer)	$V = 10$ V	$\lambda = 532$ nm, $P = 2$ W cm^{-2}	0.57	Two terminal	[139]
Exfoliated flake (10–60 nm)	$V_{ds} = 1$ V, $V_{gs} = -3$ V	$\lambda = 633$ nm, $P = 50$ mW cm^{-2}	0.12	Global bottom	[14]
Exfoliated platelet (Film)	$V = 15$ V	$\lambda =$ AM 1.5, $P = 100$ mW cm^{-2}	10^{-4}	Global bottom	[140]
Exfoliated flake (10–80 nm)	$V_{ds} = 1$ V, $V_{gs} = 8$ V	$\lambda = 532$ nm, $P = 2$ mW cm^{-2}	342.6	Local bottom	[132]

[a] Higher R value of 2200 A W^{-1} was obtained under vacuum conditions (2.5×10^{-5} mbar).
[b] Higher R value of 0.55 A W^{-1} was the result of the modified MoS_2 through laser treatment (~85 mW / 532 nm).

The averaged transmittances of the transparent TFTs and reference ITO glass in the wavelength range of 300–950 nm were estimated to be ~81% and ~87%, respectively. They were almost identical in the most sensitively responsive wavelengths to human eye (450–650 nm). However, the as-fabricated transparent TFT exhibited relatively inferior performances, (i.e. μ_{eff} of 1.4 cm^2 V^{-1} s^{-1} and I_{on}/I_{off} of ~10^3), because of the large SBH between multilayer MoS_2 and IZO S/D electrodes. To improve device performance, a picosecond pulse laser was selectively irradiated on the contact regions (see also figure 2(a)), by which μ_{eff} and I_{on}/I_{off} were increased to 4.5 cm^2 V^{-1} s^{-1} and ~10^4, respectively. These results were attributed to the increased conductivity of the interfacial side in IZO electrodes due to the oxygen deficient defects generated by laser annealing treatment [127–129].

Recently, Hong *et al* reported on another transparent multilayer MoS_2 TFT showing high device performance through the intercalation of the thin Al layer between the MoS_2 active layer with a thickness of 39.0 ± 7.4 nm and IZO S/D electrodes [130]. By careful choices of the thickness and configuration of the Al intercalting layer in the S/D electrodes, the transmission spectrum and corresponding averaged transmittance of the transparent TFT showed comparable optical behaviors with those in [126] (figure 4(b)). The μ_{eff} and I_{on}/I_{off} of the transparent TFT without the Al intercalating layer were also similar to [126]. However, those of the device with the Al layer drastically increased up to 33.6 cm^2 V^{-1} s^{-1} and ~10^7, respectively, which were mainly ascribed to the low work function of Al (4.06–4.26 eV) contributing to a distinct reduction of the SBH and contact resistance. As post-thermal treatment was not applied and thin native Al_2O_3 existed between Al and IZO due to the vacuum breaking deposition procedures, there exists a possibility of further improvement in device performance.

3.3. Opto-electronic devices: sensitive photodetectors

Photoresponsivity (R), the ratio of the photocurrent to the incident optical power [14, 131, 132], is a primary figure of merit in photo-sensing/detecting application. It has been reported that TMDs presented higher R values [14, 133–135] than that of graphene TFTs [136]. Table 2 lists the representative R values of various MoS_2 TFTs in literature reported so far [14, 134, 135, 137–140]. As can be seen in table 2, much higher R values were obtained in monolayer MoS_2 TFTs, whereas those in multilayer MoS_2 TFTs have remained less than 1 A W^{-1}. In principle, multilayer MoS_2 could be more advantageous for diverse applications than monolayer MoS_2 because of the higher DOS by about three times and the wider spectral response from the ultraviolet to near-infrared region. However, the indirect energy band structure of multilayer MoS_2 degrades photo-sensing/detecting characteristics, which is detrimental to opto-electronic applications.

In contrast to these trends, Yoon and coworkers proved that photo-detecting behaviors of multilayer MoS_2 TFTs can be significantly improved by using a local bottom-gate structure having gate underlap regions between the gate and the S/D electrodes, which was modified from the conventional bottom-gate (hereafter referred to as global bottom) TFT, as shown in figure 5 [132]. The 3D atomic force microscope image and corresponding line profile clearly demonstrate the existence of the gate underlaps. Figure 5(b) shows transfer and output characteristics of the multilayer MoS_2 TFT with the local bottom-gate structure under dark conditions. The μ_{eff} and I_{on}/I_{off} of the device were estimated to be 25.55 cm^2 V^{-1} s^{-1} and ~10^3, respectively, which were somewhat less than those of global bottom-gate structures. These results would be attributed to the parts of the multilayer MoS_2 sitting on the gate underlaps. As they were not modulated by gate bias, they might act like series resistors between the active layer and the S/D electrodes. The transfer characteristics of the same device under light illumination shown in figure 5(c) revealed the significant enhancements of the currents at both on and off states. It needs to be mentioned that photoresponsive behaviors and current enhancement were slightly observed only at the off state in case of the global bottom-gate structure [14]. When light with the power density of 64 mW cm^{-2} was illuminated on the device, the current has been increased by 3 orders of magnitude in the off state and by 2.5 times in the on state, respectively. The maximum R of 342.6 A W^{-1} was obtained at 2 mW cm^{-2} in the on state (figure 5(c)), which was remarkably higher by more than 3 orders of magnitude than the previously reported value for multilayer MoS_2 TFTs (see also table 2). The simulated R values based on the model [141] matched well with the measured R values of 14 local bottom-gate TFTs with various lengths of gate underlap (1.1–3.3 μm) and those of 14 multilayer global bottom-gate TFTs. Moreover, Kim and coworkers adopted this novel structure also to a-Si:H TFTs with different

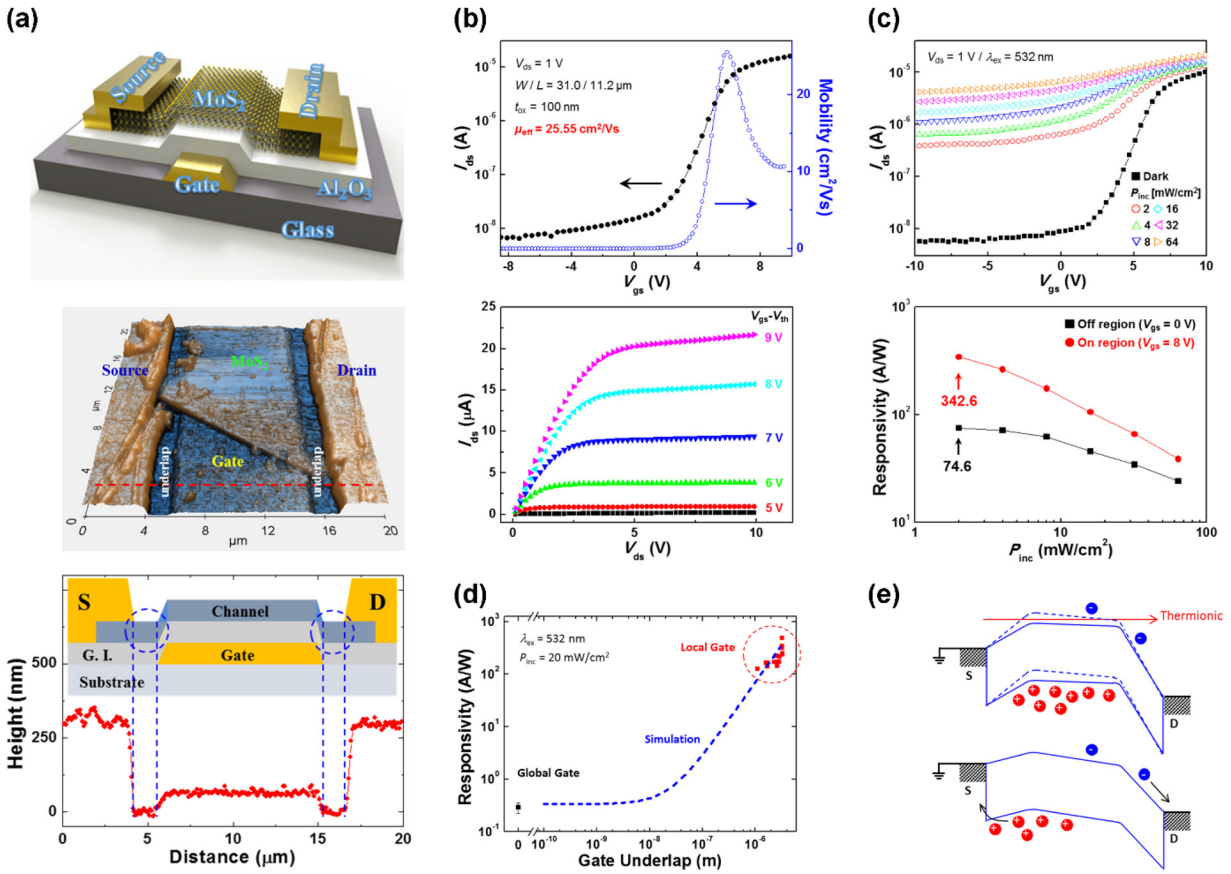

Figure 5. (a) Multilayer MoS_2 TFT with the local bottom-gate structure. (Top) 3D schematic structure of local bottom-gate TFT. (Middle) 3D AFM topographic image of the device, showing ungated MoS_2 channel regions (gate underlap) between the gate and the S/D electrodes. (Bottom) Topological line profile along the red line in the middle of (a). Inset: cross-sectional view of the device. (b) Electrical properties of the device under dark conditions. (Top) Transfer characteristic curve and μ_{eff} of the device. (Bottom) Output characteristic curves of the same device with different V_{gs}. (c) Photoresponsive behavior of a multilayer MoS_2 TFT with the local bottom-gate. (Top) Comparison of transfer characteristics under dark (solid symbol) and light conditions (open symbols) with various incident optical power densities. (Bottom) R as a function of incident power density in logarithmic scale, obtained in off ($V_{\text{gs}} = 0$ V) and on ($V_{\text{gs}} = 8$ V) regions. (d) Comparison of the simulated R line (blue dash), measured R values (red squares) of 14 local bottom-gate TFTs with various lengths of gate underlap (1.1–3.3 μm) and those of 14 multilayer global bottom-gate TFTs (black square with error bar). (e) Energy band diagram showing the effects of gate underlap. Kwon *et al* [132] John Wiley & Sons. Copyright 2015 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

dimensions of gate underlap [142]. The authors identified very analogous behaviors more quantitatively, and successfully verified the validity and materials-independent nature of the local bottom-gate structure.

4. Strategies to improve performance of TMDs TFTs

In this section, we will discuss a couple of strategies applicable to the devices described in section 3 to boost the overall performance. First, we start with the recent progresses to improve contact properties with TMDs. Then, we discuss hybridizing strategies based on the combinations of 2D materials. Finally, we briefly review a couple of chemical doping techniques in terms of dipole or charge transfer.

4.1. Contact between active material and S/D electrodes

As most metals form Schottky contacts to TMD 2D materials, the SB introduces large contact resistance to the device. However, to realize high performance TMD TFTs, low contact resistance is critical.

Low work function metals are widely used as contacts to TMD materials. Das *et al* presented a thorough experimental study of contacts to multilayer MoS_2 utilizing low work function metals such as scandium (Sc) and Ti to lower the contact resistance and improve the electron injection for n-type MoS_2 TFTs [27]. Density-functional theory calculation and experiment reveal that the SBH at the Mo and MoS_2 junction is as low as ~0.1 eV indicating the high quality of the Mo/MoS_2 contact interface [143, 144]. Furthermore, indium and Ti are also used to form Ohmic contacts to monolayer tungsten diselenide (WSe_2) [32, 145]. However, a number of recent articles report that using large work function metals such as nickel (Ni), Au, and platinum (Pt) also can realize excellent n-type contacts (figure 6(a)) [7, 27, 146]. This was attributed to the effect of the Fermi level pinning at the MoS_2/metal interface near the conduction band of the MoS_2 [147, 148]. Alternatively, substoichiometric molybdenum trioxide (MoO_{3-x}), which is a high work function material, was

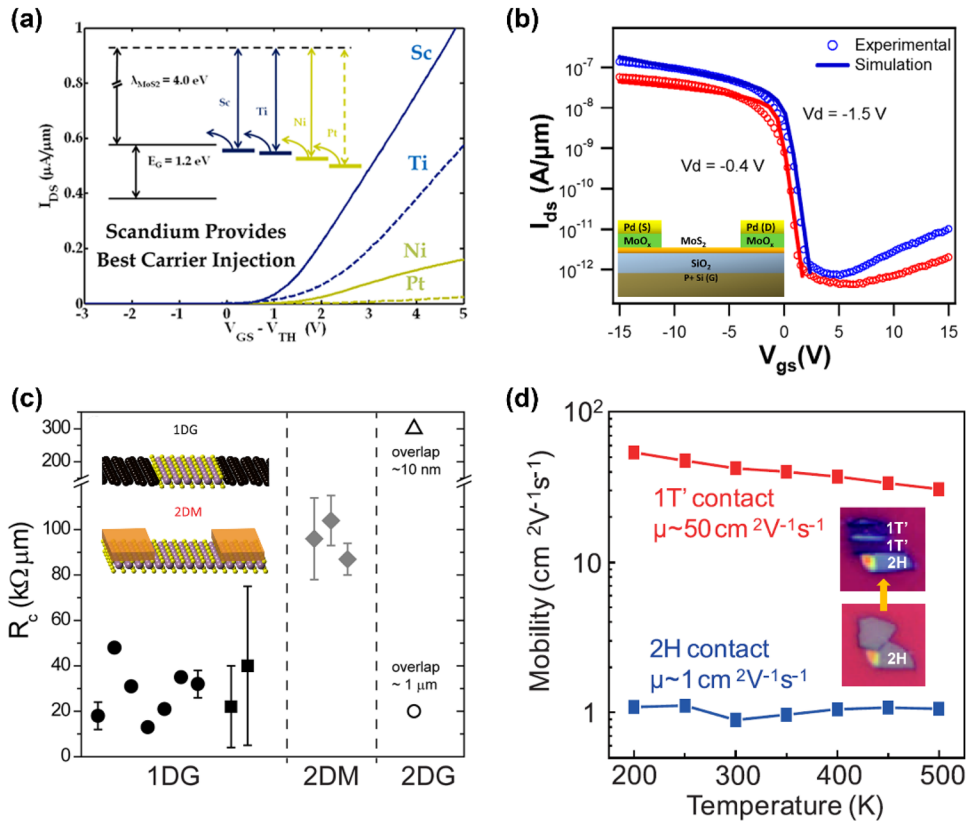

Figure 6. (a) Transfer characteristics of MoS_2 TFTs with Sc, Ti, Ni, and Pt metals contacts. Inset: actual line-up of metal Fermi level with the electronic bands of MoS_2. Reprinted with permission from [27]. Copyright 2013 American Chemical Society. (b) Transfer characteristics of a MoS_2 TFT with MoO_{3-x} contact. Inset: schematic cross-sectional structure of the MoS_2 TFT. Reprinted with permission from [123]. Copyright 2014 American Chemical Society. (c) Contact resistance values for different devices at high carrier density: the solid circles (squares), gray diamonds and open symbols represent MoS_2 (WS_2) devices with 1D graphene contacts, 2D metal contact to MoS_2 and devices with 2D graphene contacts, respectively. Reprinted with permission from [151]. Copyright 2016 American Chemical Society. (d) μ_{eff} of the 2H $MoTe_2$ TFTs with 2H and 1T contacts as a function of temperature. From [155]. Reprinted with permission from AAAS.

used as hole contacts in MoS_2 TFTs (figure 6(b)) [123]. The MoO_{3-x}/MoS_2 contact interface shows a lower degree of Fermi level pinning as compared to the metal/MoS_2 contact interface.

Various innovative approaches to reduce the contact resistance have also been reported. Graphene contact to TMDs can significantly reduce the Fermi level pinning because of the reduced interface states [124, 149, 150]. The electronic coupling between metal contact and MoS_2 can be enhanced by inserting graphene, and such a graphene/metal hetero-contact can also reduce the contact resistance. In addition, Guimarães *et al* reported that lateral contact of graphene to monolayer MoS_2 and tungsten disulfide (WS_2) at the edge forms Ohmic contact (figure 6(c)) [151]. To intervene an oxide layer, such as tantalum pentoxide, between MoS_2 and metal contact can also reduce the contact resistance and increase the on-current [152]. It is known that lithium compounds lead to a phase transformation of MoS_2 from 2H to 1T phase [153]. Kappera *et al* utilized the phase-transformed metallic 1T MoS_2 as the S/D electrodes and the mechanically exfoliated intrinsic 2H MoS_2 as the channel in FETs [154]. The locally patterned 1T phase MoS_2 forms Ohmic contacts to the 2H phase MoS_2 decreasing contact resistance and enhancing TFT performances. Using laser irradiation, the molybdenum ditelluride ($MoTe_2$) phase transforms from semiconducting 2H to metallic 1T [155]. Because the energy difference between the two phases is very small, stable homo-junctioned contacts can be formed at the interface between 2H and 1T $MoTe_2$, which greatly improves the device performance (figure 6(d)).

Yu *et al* first reported the large-scale monolayer MoS_2-graphene hybrid structure using MoS_2 as the active layer and graphene as contact electrodes, respectively [156]. Figure 7 shows the electrical properties of MoS_2-graphene and MoS_2–Ti TFTs. The output characteristic of the MoS_2-graphene TFTs indicates that the contact between graphene and MoS_2 exhibits Ohmic behaviors, as shown in figure 7(a). Transfer characteristics of MoS_2-graphene and MoS_2-Ti TFTs show that they both have high I_{on}/I_{off} of ~10^6, as can be seen in figures 7(b) and (d). However, the μ_{eff} of MoS_2-graphene TFTs (17 cm^2 V^{-1} s^{-1}) can be higher than that of MoS_2–Ti TFTs (1.8 cm^2 V^{-1} s^{-1}), as shown in figure 7(c). Furthermore, the contact resistances extracted from the current–voltage ($I - V$) characteristics of MoS_2-graphene and MoS_2–Ti TFTs were estimated to be 0.1 and 1 kΩmm, respectively. In the MoS_2–Ti structure, SBH does not change because it was determined by the energy difference between the work function of the Ti and the electron affinity of the MoS_2. However, the SBH of MoS_2-graphene TFTs dramatically decreases with increasing V_{gs}, as shown in figure 7(e). This is consistent with previous studies, showing the SBH of MoS_2-graphene ranging from 22 meV to 260 meV [114, 157]. As a result, unlike MoS_2–Ti TFTs,

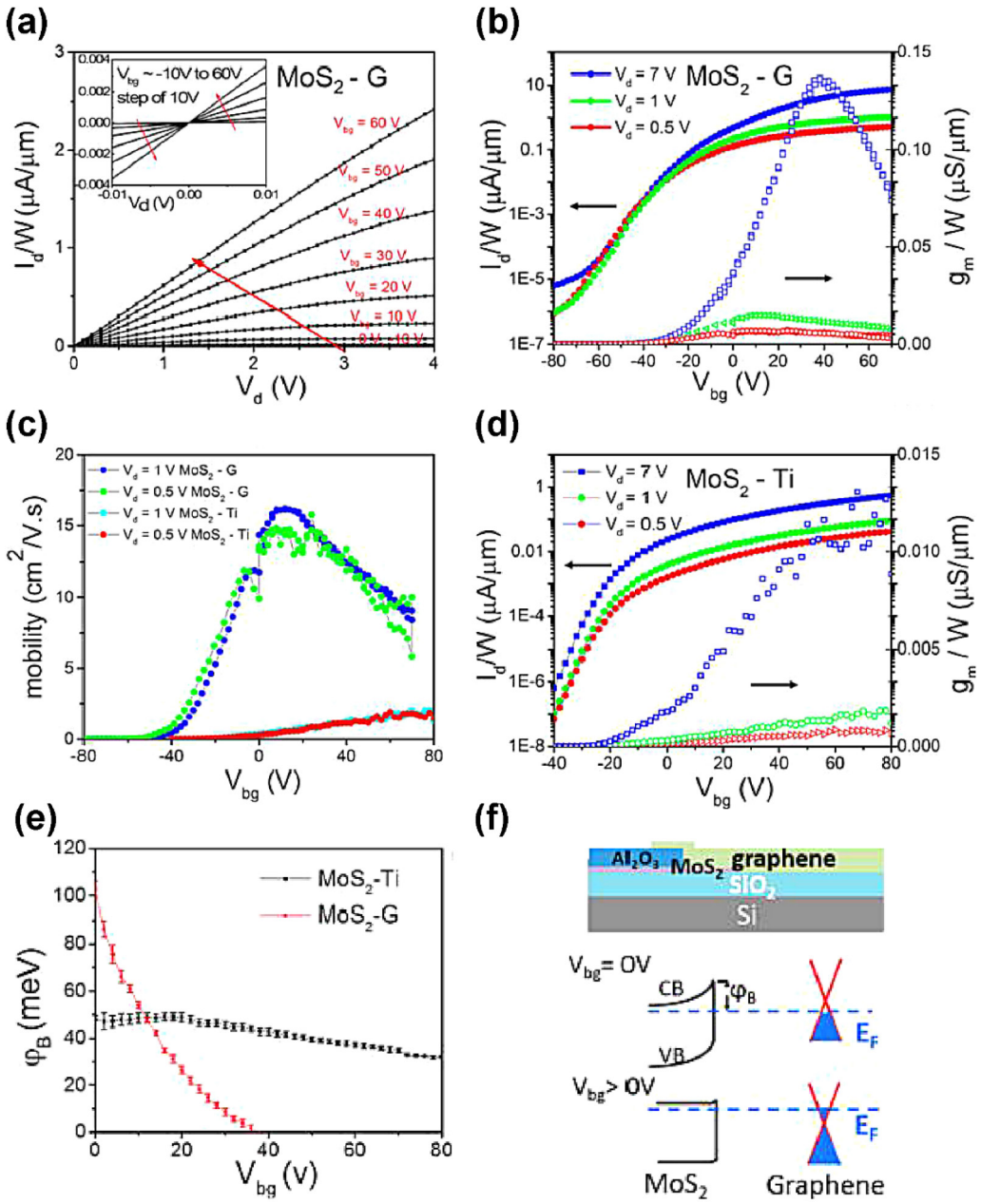

Figure 7. Bottom-gated transport properties of MoS_2-graphene and MoS_2–Ti TFTs performance at RT. (a) Output performances of a representative MoS_2-graphene TFT at large field and small field with both negative and positive biases (inset). (b) Transfer characteristics of MoS_2-graphene TFT on the left axis and transconductance on the right axis. (c) μ_{eff} as a function of V_{gs} in MoS_2-graphene and MoS_2–Ti TFTs at different V_{ds}. (d) Same as in (b) for the control system MoS_2–Ti. (e) SBH and corresponding error bars, as a function of the V_{gs} for CVD-grown MoS_2-graphene and MoS_2–Ti junctions. (f) (Top) Experimental setup. (Bottom) Schematic energy band diagram of the MoS_2-graphene heterostructure at $V_{gs} = 0$ and $V_{gs} > 0$. Reprinted with permission from [156]. Copyright 2014 American Chemical Society.

figure 7(f) shows that the SBH of MoS_2-graphene changes depending on V_{gs}.

4.2. TMD heterostructures

Gong *et al* reported a one-step growth method for the high quality vertical and in-plane WS_2/MoS_2 heterostructure [158]. The vertically stacked WS_2/MoS_2 heterostructure was synthesized at a high temperature (~850 °C). The TFTs fabricated from vertically stacked WS_2/MoS_2 has a high I_{on}/I_{off} of ~10^6, and the μ_{eff} was estimated to be from 15 to 34 $cm^2\,V^{-1}\,s^{-1}$. The μ_{eff} of the CVD grown WS_2/MoS_2 heterostructure TFTs was much higher than those of monolayer MoS_2 (4.5 $cm^2\,V^{-1}\,s^{-1}$), bilayer MoS_2 (5.7 $cm^2\,V^{-1}\,s^{-1}$), and the transferred WS_2/MoS_2 (0.51 $cm^2\,V^{-1}\,s^{-1}$) [159, 160]. Compared with the transferred WS_2/MoS_2 heterostructure, the CVD grown WS_2/MoS_2 heterostructure has a clean interface between the WS_2 and MoS_2 layer. On the other hand, the WS_2/MoS_2 in-plane heterostructure, which was obtained at 650 °C, exhibited a good rectifying behavior. This indicates that WS_2/MoS_2 heterostructures

form intrinsic monolayer $p-n$ junctions without external bias, because monolayer MoS_2 and WS_2 exhibit n- and p-type semiconducting behaviors, respectively.

Graphene, hBN and TMDs provide a full range of material types including semimetals, large band gap insulators, and semiconductors. The van der Waals heterostructures formed by stacking these 2D materials can exhibit outstanding electronic as well as photonic properties. Britnell *et al* demonstrated a prototype tunneling FET consisting of a vertically stacked graphene/six-layer MoS_2/graphene structure with hBN encapsulating layers [161]. The devices exhibited the switching ratio of ~10^4 with much faster transition time than planar FETs at room temperature (RT). Georgiou and co-workers reported on graphene/few-layer WS_2/graphene tunneling FET structures, where WS_2 acted as a tunnel barrier [162]. The small band gap of WS_2 allows the switch between tunneling and thermionic transport regimes, leading to a large on current and high I_{on}/I_{off} over 10^6. Yu *et al* and Moriya *et al* reported on similar vertical FETs with graphene/multilayer MoS_2/metal heterostructures [157, 163]. The former group got I_{on}/I_{off} of ~10^3 and current density as high as 5000 A cm^{-2} at RT [157]. The latter group realized a better interface between graphene and MoS_2 by replacing the CVD-grown graphene with an exfoliated one [163]. They further improved I_{on}/I_{off} to 10^5 and current density in on state ~10^4 A cm^{-2}. The interface between graphene and MoS_2 exhibits SB, which can facilitate strong current rectification. Roy and co-workers fabricated an all-2D transistor using few-layer MoS_2 as the channel material, hBN as the top-GI, and graphene as S/D and gate electrodes [164]. The transistor showed n-type behavior with I_{on}/I_{off} over 10^6 and μ_{eff} of ~33 cm^2 V^{-1} s^{-1}.

The photodetectors with various 2D heterostructures were also demonstrated. Roy and co-workers reported a graphene/multilayer MoS_2 heterostructure with R higher than 10^8 A W^{-1} at RT [165]. Through electric field tuning, the device also exhibits persistent photoconductivity, which can act as highly sensitive gate-tunable photodetectors and optical switches. Britnell *et al* demonstrated a photodetector consisting of graphene/multilayer WS_2/graphene heterostructures [166]. This vertically stacked device was also realized on a flexible PET substrate, which exhibited R above 0.1 A W^{-1} and an external quantum efficiency (EQE) over 30%. Yu and co-workers presented a high efficient photodetector with graphene/MoS_2/graphene heterostructures [167]. A maximum R is estimated to be ~0.22 A W^{-1}, corresponding to an EQE of 55%. Cheng *et al* reported on a vertical p–n diode based on p-type monolayer WSe_2 and n-type multilayer MoS_2, respectively [168]. The atomically thin p–n diode shows rapid photoresponsive behaviors on the entire overlapping area with a maximum EQE of 12%. Deng *et al* stacked exfoliated few-layer BP on CVD-grown monolayer MoS_2 in order to form a p–n heterojunction [169]. Upon 633 nm laser illumination, this BP/MoS_2 p–n diode exhibits R of 418 mA W^{-1} and an EQE of 0.3%.

Although the mechanical transfer method provides high crystallinity 2D flakes and high quality interfaces, the issues of relatively small dimension and locating control still need to be resolved. Recently, the CVD technique shows a great potential in the direct growth of patternable 2D building blocks to fabricate van der Waals heterostructures with upscaling at desirable positions. Choudhary *et al* reported on large-area and patterned 2D heterostructures with a vertical stack using CVD grown MoS_2 and WS_2 [170]. In addition, a flexible diode was also fabricated by transferring the MoS_2/WS_2 film onto a PET substrate showing a current ratio over 10^3. Xue *et al* also produced patterned few-layer WS_2/MoS_2 vertical heterojunction arrays by separate deposition of tungsten oxide and Mo, followed by sulfurization, respectively [171]. The photodetectors fabricated by using the MoS_2/WS_2 heterojunction arrays exhibited R of 2.3 A W^{-1}. The authors claimed that their photodetector could be self-driven without applying S/D bias, which was attributed to a built-in electric field at the interface of the MoS_2/WS_2 heterojunction. Lin and co-workers demonstrated that CVD-grown epitaxial graphene were used as a growth template for MoS_2, WSe_2, and hBN, which could be assembled into large-scale van der Waals heterostructures [172]. It was found that the residues, strains, and wrinkles on the surface of graphene play a role of a nucleation site for the lateral growth of the overlayers. The R obtained from the MoS_2 directly grown on epitaxial graphene was 10^3 times higher than the bare MoS_2.

4.3. Chemical doping

Conventional doping of an inorganic semiconductor is accomplished by substituting impurities (dopants) with different valence electrons for atoms in the host semiconductor. Ion implantation followed by thermal treatment has been most commonly utilized in the substitutional doping technique. However, substitutional doping is quite a slow procedure and can only be achieved during bulk crystal growth, which might be hard to apply after fabricating (opto-)electronic devices, especially flexible ones. Recently, many research groups have reported on the substitutional doping of TMDs by using niobium [173], iron [174], manganese [175], other transition metals [176, 177], and phosphorus [178] etc.

On the other hand, doping in organic semiconductors with a π-conjugated structure exhibits quite distinct characteristics compared with inorganic semiconductors. Dopant atoms or molecules are intercalated between adjacent π-conjugation paths in host organic materials resulting in the steric deformation of host lattices as well as charge transfer phenomena from host to dopant. Polarity of the doped organic materials is determined by the type of dopant (i.e. electron donor or acceptor). This intercaltional or charge transfer doping is conducted at a relatively low temperature based on solution process or gaseous environments [179], which could easily apply to the fabricated devices through simple spin-coating or gas-exposure. From these points of view, charge transfer doping has been explosively investigated in 2D materials including TMDs. For n-type doping, various reducing reagents, such as ammonia [180], amines [181], tetrathiafulvalene [182], alkali metals [183], benzyl viologen [184], and nicotinamide adenine dinucleotide [185] etc have been utilized. Oxidizing dopants,

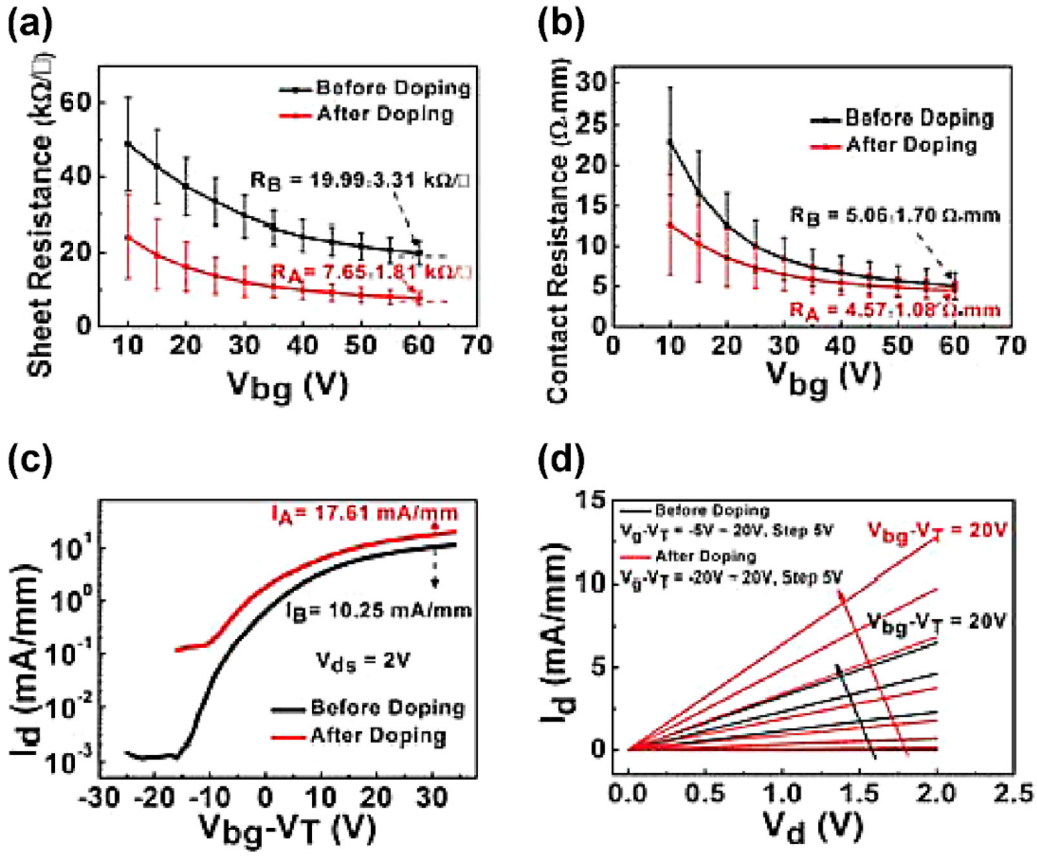

Figure 8. (a) Comparison of sheet resistance before and after PEI doping as a function of V_{gs}. (b) Comparison of contact resistance before and after PEI doping with different V_{gs}. (c) Transfer characteristics of TFT with $L = 3$ μm before and after PEI doping at $V_{ds} = 2$ V. (d) Output characteristics of the same device before and after PEI doping. Reproduced with permission from [191]. Copyright 2013 IEEE.

for example water [186], oxygen [187], nitrogen monoxide [188], nitrogen dioxide [31], gold(III) chloride [189], MoO_3 [190], and tetracyanoquinodimethanes [185], induced *p*-type doping in various 2D materials.

Du *et al* compared the device performance of MoS_2 TFTs before and after polyethylenimine (PEI) molecule doping, as shown in figure 8 [191]. Figure 8(a) shows the sheet resistance of the MoS_2 TFTs before and after PEI doping. Compared with the pristine TFT, the PEI-doped one showed reduced sheet resistance by ~2.6 times due to electron transfer from PEI molecules to the MoS_2 layers. The contact resistance at the Ti-MoS_2 interface is also decreased by ~20% after PEI doping (figure 8(b)). As a result, figures 8(c) and (d) show that PEI treatment clearly enhances the transfer and output characteristics of the MoS_2 TFTs. After PEI doping, the V_{th} shifts to the negative direction with respect to that of the pristine device. It means that PEI molecules act as *n*-type dopants. PEI doping also improves μ_{eff} extracted from transfer curves. Besides, Hafiz *et al* [192] and Lingming *et al* [193] reported similar results, stating that the chemical doping, such as the lithium fluoride (LiF) and the chlorine (Cl), remarkably improve the electrical properties of the TMD TFTs. After chemical doping, sulfur vacancy could be substituted with fluorine or Cl atoms in the TMDs. Contact resistance is reduced because the chemical dopants act as electron donors.

5. Concluding remarks

We reviewed recent studies on high-mobility TFTs built on multilayer TMDs and other 2D materials. Great research effort has been made on the fabrications and measurements of 2D material transistors. Flexible and/or transparent TFTs with 2D semiconductors are promising for future flexible electronics and transparent displays. In addition, TMD photodetectors with local bottom-gate structures can provide high photoresponsivity. The contact resistance of TMD devices can be reduced by choosing low work function metals, metal oxides, graphene, and phase transformed metallic TMDs. Furthermore, the 2D heterostructures and chemical doping can also enhance the carrier mobility of TFTs. It is expected that multilayer 2D material transistors find their way to real-life applications in the form of various high-performance electronics.

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