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Asymmetric Double-Gate β-Ga_2O_3 Nanomembrane Field-Effect Transistor for Energy-Efficient Power Devices

*Jiyeon Ma, Hyung Jun Cho, Junseok Heo, Sunkook Kim, and Geonwook Yoo**

The ultra-wide bandgap and cost-effective melt-growth of β-Ga_2O_3 ensure its advantages over other wide bandgap materials, and competitive electrical performance has been demonstrated in various device structures. In this paper, an asymmetric double-gate (ADG) β-Ga_2O_3 nanomembrane field-effect transistor (FET) comprised of a bottom-gate (BG) metal-oxide field-effect transistor and a top-gate (TG) metal-semiconductor field-effect transistor (MESFET) is demonstrated. Schottky contact properties are validated by characterizing the lateral Schottky barrier diode (SBD), which exhibits high rectification ratio and low ideality factor. The top-gate β-Ga_2O_3 MESFET shows reasonable electrical performance with a high breakdown voltage, as anticipated by three terminal off-state breakdown measurement. These properties are further enhanced by double-gate operation, and superior device performance is demonstrated; positive-shifted threshold voltage and reduced subthreshold slope enable the asymmetric double-gate β-Ga_2O_3 FET to operate at low power, and almost twice as much transconductance is demonstrated for high-frequency operation. These results show the great potential of asymmetric double-gate β-Ga_2O_3 FETs for energy-efficient high-voltage and -frequency devices with optimal material and structure co-designs.

1. Introduction

Beta-gallium oxide (β-Ga_2O_3) has attracted great attention in recent years due to its superior electrical properties for next generation power electronics; ultra-wide bandgap estimated to be about 4.6–4.9 eV allows high-temperature and high-voltage operation with an estimated large breakdown field (E_{br}) of up to 8 MV cm^{-1}.[1–3] Therefore, β-Ga_2O_3 possesses high Baliga's figure-of-merit (FOM) used for evaluating applicability of a material to power device performance, and the estimated FOM is several times higher than that of current viable solutions such as silicon carbide (SiC) and gallium nitride (GaN).[4,5] In addition, cost-effective high quality β-Ga_2O_3 wafer from bulk single crystal obtained from melt-growth methods provides a significant advantage over other wideband gap materials because SiC and GaN wafers require expensive high temperature vacuum synthesis.[6–9] Furthermore, β-Ga_2O_3 exhibits a comparable Johnson FOM intended for high-frequency operation in spite of its relatively lower saturation velocity.[10,11]

Aforementioned unique properties of β-Ga_2O_3 have facilitated intensive research efforts for high-power and radio-frequency (RF) electronics, and various device structures have been demonstrated as a building block such as Schottky barrier diode (SBD), metal-oxide field-effect transistors (MOSFET), metal-semiconductor field-effect transistors (MESFET), and even heterostructures with low dimensional materials.[12–16] In particular, MESFET not only eliminates problems with oxide reliability and interface traps but also provides better size scaling, and thus β-Ga_2O_3 MESFET is a promising structure for the applications.[6,17] On the other hand, back- and top-gate modulation of β-Ga_2O_3 MOSFET is reported, showing that the electrical characteristics can be beneficially tuned.[18]

In this work, we fabricate asymmetric double-gate (DG) β-Ga_2O_3 nanomembrane FET having bottom-gate (BG) MOSFET and top-gate (TG) MESFET. Specifically, a high crystal quality β-Ga_2O_3(100) channel is obtained from a bulk β-Ga_2O_3 crystal substrate using a mechanical exfoliation method. The asymmetric DG β-Ga_2O_3 FET is comprised of a lateral Schottky barrier diode, BG-MOSFET, and TG-MESFET, which are characterized separately to validate and compare their electrical performance. Benefiting from performance modulations of the individual devices, high performance asymmetric DG β-Ga_2O_3 FET is achieved for energy-efficient high voltage and frequency devices. Moreover, detailed analysis has been conducted to assess the modulation of electrical properties as well as enhanced performance based on energy band model and TCAD simulations.

2. Results and Discussion

Figure 1a,b presents a schematic illustration and optical microscope image of the fabricated asymmetric DG β-Ga_2O_3 field-effect transistor. The length between gate and source (L_{GS}) and

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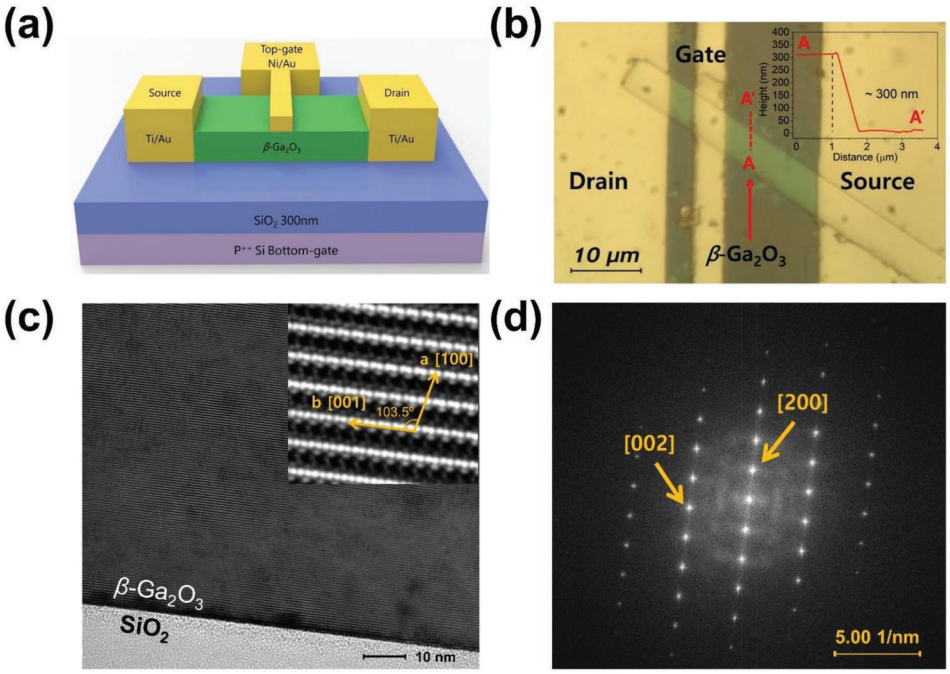

Figure 1. a) Schematic illustration and b) optical microscopy image of the fabricated double-gate β-Ga_2O_3 nanomembrane field-effect transistor. (c) HR-TEM image of the exfoliated β-Ga_2O_3 nanomembrane onto SiO_2 with the indication of calculated angle. (d) Electron diffraction pattern of a selected area confirming the surface orientation of (100).

between gate and drain (L_{GD}) are 13.7 and 3.7 µm, respectively, and the channel thickness of ≈300 nm is confirmed. A cross-sectional high resolution transmission electron microscopy (HR-TEM) images of β-Ga_2O_3/SiO_2 in Figure 1c show the smooth interface between β-Ga_2O_3 and SiO_2, indicating that clear transfer onto SiO_2 is achieved without faults and the exfoliated flake preserves high crystal quality of bulk crystal with no damage or strain. The calculated angle (β = 103.5°) confirms [100] and [001] direction.[19] This facile and clean cleavage along the [100] direction can be achieved due to a monoclinic crystal structure having a much larger lattice constant in the [100] direction. Figure 1d shows the selected-area electron diffraction pattern revealing the lattice constants and directions of the β-Ga_2O_3 flake by calculating d-spacing; the β-Ga_2O_3(100) crystal plane on the channel surface is confirmed.[20] Although the mechanical exfoliation method is not a scalable approach, it preserves high crystal quality of β-Ga_2O_3 and allows to investigate electrical performance in various device structures.

Schottky contact properties of the TG metal (Ni/Au) on β-Ga_2O_3(100) channel is studied by characterizing a lateral Schottky barrier diode (SBD); **Figure 2**a shows its semi-logarithmic *I–V* characteristics with a schematic diagram. The Schottky contact between Ni and β-Ga_2O_3 is associated with work function difference (Nickel: 5.04–5.35 eV, β-Ga_2O_3: 4.11 eV).[21] The ohmic contact (D) is grounded as a cathode, and a sweeping bias is applied to the TG as an anode. Other

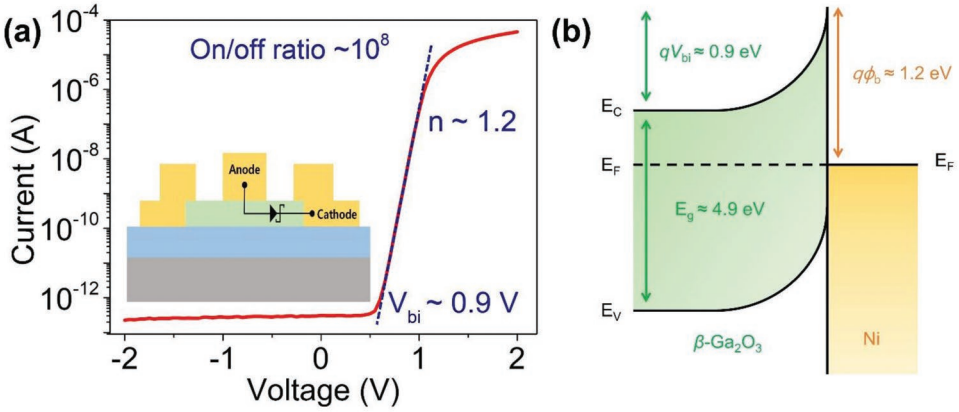

Figure 2. a) *I–V* characteristics of the Ni/β-Ga_2O_3 Schottky barrier diode (SBD). (Inset) Cross-sectional schematic of the SBD with its symbol. b) Band diagram of the Ni/β-Ga_2O_3 Schottky contact with calculated parameters.

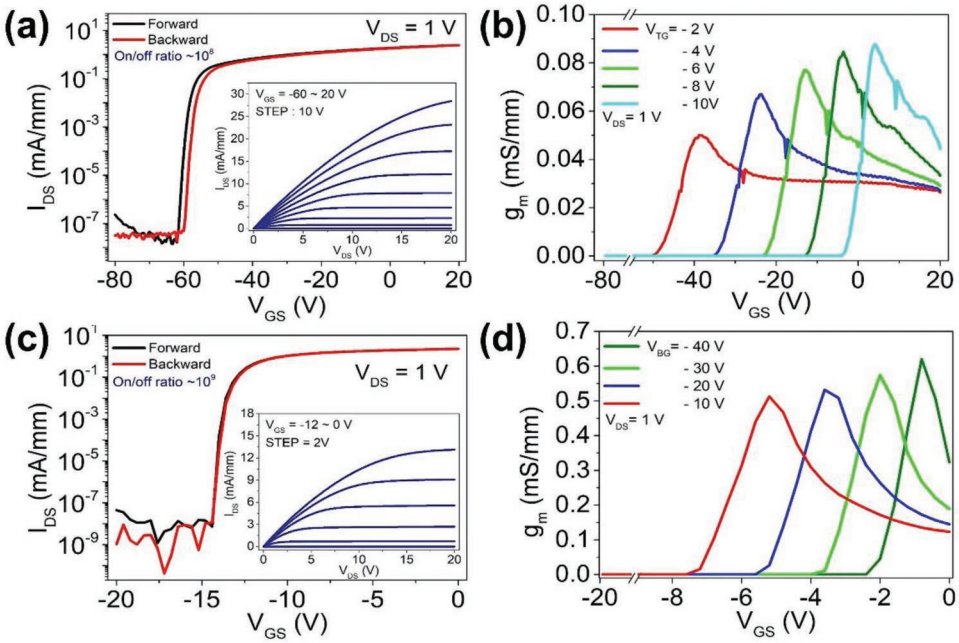

Figure 3. a) Hysteretic transfer curves (I_{DS}–V_{GS}) of the fabricated BG β-Ga_2O_3 MOSFET with floating TG at V_{DS} = 1 V (Inset) Output curves (I_{DS}–V_{DS}) from V_{GS} –60 to 20 V with 10 V step. b) Evolution of g_m–V_{GS} curves at V_{DS} = 1 V under opposite V_{TG} from –10 to –2 V with 2 V step. c) Hysteretic transfer curves (I_{DS}–V_{GS}) of the fabricated of the fabricated TG β-Ga_2O_3 MESFET with floating BG at V_{DS} = 1 V. (Inset) Output curves (I_{DS}–V_{DS}) from V_{GS} –60 to 20 V with 10 V step. d) Evolution of g_m–V_{GS} curves at V_{DS} = 1 V under opposite V_{BG} from –40 to –10 V with 10 V step.

contact behaviors under different configurations are shown in Figure S1, Supporting Information. The SBD exhibits high rectification ratio of ≈10^8, and additional parameters are extracted using $I = I_S\left(exp\left(\frac{qV}{nkT}\right)\right) - 1$, where q is the electronic charge, V is the forward bias, n is ideality factor, k is the Boltzman constant, T is the absolute temperature.[22] The built-in potential (V_{bi}) of ≈0.9 V and ideality factor (n) of ≈1.2 are extracted from a linear extrapolation method. The Schottky barrier height ($q\phi_B$) of 1.2 eV is also calculated from $\phi_B = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_S}\right)$, where A is the area, and A^*, the Richardson constant is 41.1 A $cm^{-2}\cdot K^2$ at room temperature.[23,24] The corresponding energy band diagram of Ni/β-Ga_2O_3 (100) Schottky contact is established in Figure 2b.

Figure 3a shows hysteretic transfer curves (I_{DS}–V_{GS}) of the fabricated BG β-Ga_2O_3 MOSFET with floating TG and output curves (I_{DS}–V_{DS}) with good current saturation as well as ohmic contact behavior at low V_{DS} region in the inset. Threshold voltage (V_{TH}) of –57.7 V is calculated using a linear extrapolation method in a linear regime (at V_{DS} = 1 V) and the amount of hysteresis (ΔV) is 2.0 V. Maximum transconductance (g_m) of 0.05mS mm^{-1} and subthreshold slope (SS) of 470 mV per dec are extracted using $SS = \frac{\partial V_{GS}}{\partial(\log_{10} I_{DS})}$ and $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$, respectively. Moreover, the field-effect mobility (μ_{FE}) is ≈102 $cm^2V^{-1}s^{-1}$ which is extracted using $\mu_{FE} = \left(\frac{L}{W}\right)\cdot\left(\frac{g_{max}}{C_{BOX}\cdot V_{DS}}\right)$, where L is channel length, W is channel width, d is channel thickness, g_{max} is maximum transconductance, and C_{BOX} is SiO_2 capacitance. It is noted that positive V_{TH} shift of 25.6 V and enhanced g_m of 1.6 times were observed after depositing the TG metal (Ni/Au) on the β-Ga_2O_3 channel while SS was degraded from 180 to 470 mV per dec as shown in Figure S2, Supporting Information. Depleted region on the β-Ga_2O_3 surface induced by the Schottky contact makes the effective channel thickness thinner, resulting in positive V_{TH} shift.[25,26] Figure 3b shows the evolution of g_m-V_{GS} characteristics at V_{DS} = 1 V by applying opposite V_{TG} from –2 to –10 V with 2 V step. The max. g_m can be enhanced gradually through the TG bias effect. More details will be discussed in the following based on energy band diagram model and physics-based TCAD Sentaurus simulation.

Similarly, we characterized the fabricated TG β-Ga_2O_3 MESFET. Figure 3c shows the transfer curves (I_{DS}–V_{GS}) with negligible hysteretic behavior (ΔV = 0.02 V) with floating BG, and output curves (I_{DS}–V_{DS}) with good current saturation in the inset of Figure 3c. Positively shifted V_{TH} of –13.2 V, reduced SS of 130 mV per dec and significantly enhanced max. g_m (0.68 mS mm^{-1}) were obtained in comparison to the BG β-Ga_2O_3 MOSFET. The nearly zero ΔV implies that interface traps between Ni and β-Ga_2O_3 are successfully eliminated. The evolution of g_m–V_{GS} curve at V_{DS} = 1 V by applying V_{BG} from –40 to –10 V with 10 V step is shown in Figure 3d, and max. g_m of TG-MESFET can be further enhanced by the BG bias effect. The μ_{FE} is ≈153 $cm^2V^{-1}s^{-1}$, and this is extracted using β-Ga_2O_3 capacitance (C_S) instead of C_{BOX}, in the equation, where $C_S = \varepsilon_s/d$, ε_s is a dielectric constant of β-Ga_2O_3, and d is the channel thickness.[27] Although the Schottky contact TG would leave only limited margin to the gate-bias, the electrical performance as summarized in **Table 1** is significantly better compared with β-Ga_2O_3 MOSFET structure.

Table 1. Summary of the characterized electrical performance.

$V_D = 1$ V	$g_{m\ (max)}$ [mS mm^{-1}]	μ_{FE} [cm^2 V^{-1}·s^{-1}]	V_{TH} [V]	*SS* [mV per dec]	ΔV [V]	On/off
BG-MOSFET	0.05	102	−57.7	470	2	$1.7 \cdot 10^8$
TG-MESFET	0.36	153	−13.2	130	0.02	$1.9 \cdot 10^9$
ADG-FET	0.68	184	−7.1	110	0.05	$1.2 \cdot 10^9$

Bottom-gate (BG) β-Ga_2O_3 MOSFET, top-gate (TG) β-Ga_2O_3 MESFET, and asymmetric double-gate (DG) β-Ga_2O_3 FET.

Energy band diagram model is proposed and related TCAD simulations are performed to describe the observed V_{TH} shift and improved g_m. **Figure 4**a shows the energy band diagram after the TG (Ni/Au) metal contact deposition. For the BG MOSFET shown in Figure 4b, applied negative V_{TG} bias expands the depletion width induced by Ni Schottky contact further into the β-Ga_2O_3 channel and thus reduces effective channel thickness. Corresponding carrier density distribution underneath the TG region is presented in Figure 4d. On the other hand, Figure 4c depicts energy band of β-Ga_2O_3 MESFET showing upward band bending at SiO_2/β-Ga_2O_3 interface under negative V_{BG} bias, and the corresponding carrier distribution is also shown in Figure 4e. As compared in Figure 4f, therefore, the MESFET has thinner effective channel thickness with higher peak carrier density.

To evaluate the potential of the fabricated β-Ga_2O_3 MESFET for power device application, we performed three terminal off-state breakdown measurements. **Figure 5**a shows a measured result under off-state gate bias ($V_{GS} = -15$ V) from the TG-MESFET operation in comparison with the afore-discussed output characteristics; The p^{++}-Si BG is floated during the measurement. Although gate leakage current via the Schottky contact as well as charging/discharging of the traps states results in the increased off-state drain leakage current as shown in Figure 5b, a destructive hard breakdown is not observed in our measurement setup of V_{DS} up to 210 V. Additional extended breakdown measurement exhibits BV of 293 V as shown in Figure S3, Supporting Information. The result indicates that the β-Ga_2O_3 nanomembrane TG-MESFET is promising for high power devices.

Last, we evaluate electrical performance of the proposed asymmetric DG (ADG) β-Ga_2O_3 FET by modulating both gate-bias simultaneously. **Figure 6**a,b shows transfer curves (I_{DS}–V_{GS}) and g_m–V_{GS} curves at $V_{DS} = 1$ V of the asymmetric DG β-Ga_2O_3 FET compared with TG MESFET; V_{TH} further shifts toward positive direction by the amount of $\Delta V_{TH} = 6.1$ V, and the max. g_m (0.68 mS per ss) was improved by 1.9 times, and the μ_{FE} of ADG-FET increased to ≈184 cm^{2}V^{-1}s^{-1}. A total capacitance (C_{OX}) value of two parallel capacitors ($C_S//C_{BOX}$) is used for the mobility extraction.[28] Figure 6c directly compares the output characteristics of I_{DS}–V_{DS} for the same gate-bias conditions, showing a reduced on-resistance and thus increased I_{DS} under DG operation. Furthermore, the max. g_m is further

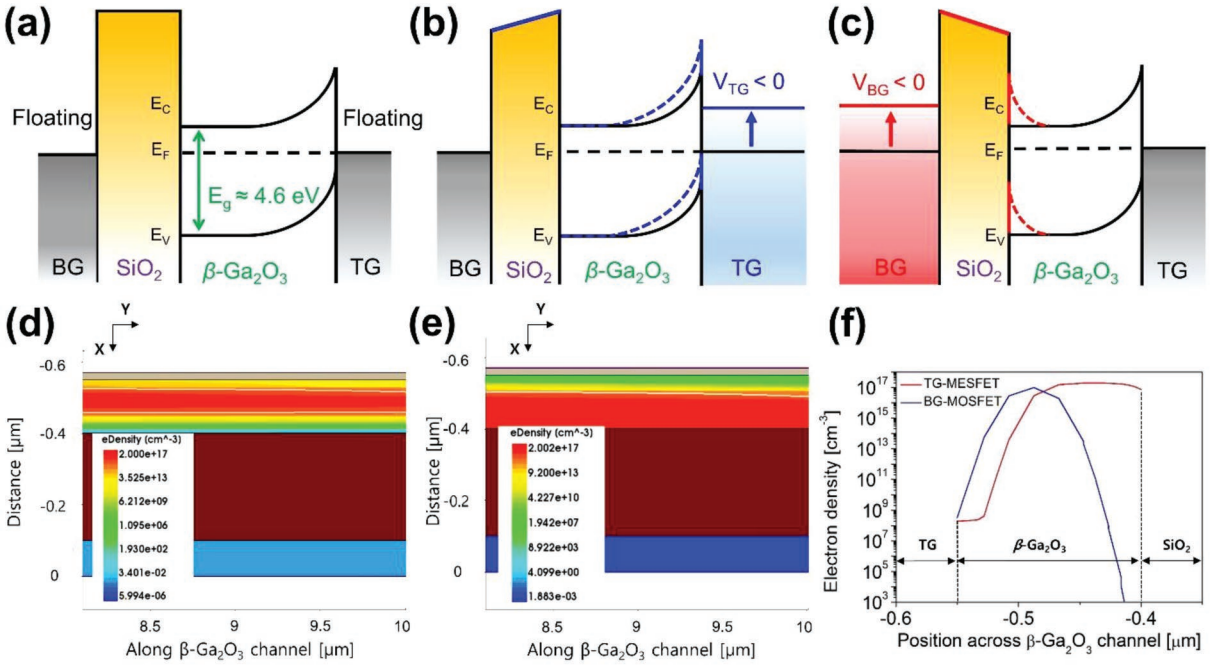

Figure 4. a) Band diagram of asymmetric double-gate β-Ga_2O_3 nanomembrane field-effect transistor with both floating BG and TG. Band diagram of b) BG MOSFET under negative TG and c) TG MESFET under negative BG. Simulated on-state electron density (eDensity) maps of d) BG MOSEFET and e) TG MESFET; f) their direct comparison across the β-Ga_2O_3 channel at the same effective gate-bias (V_{GS}–V_{TH}).

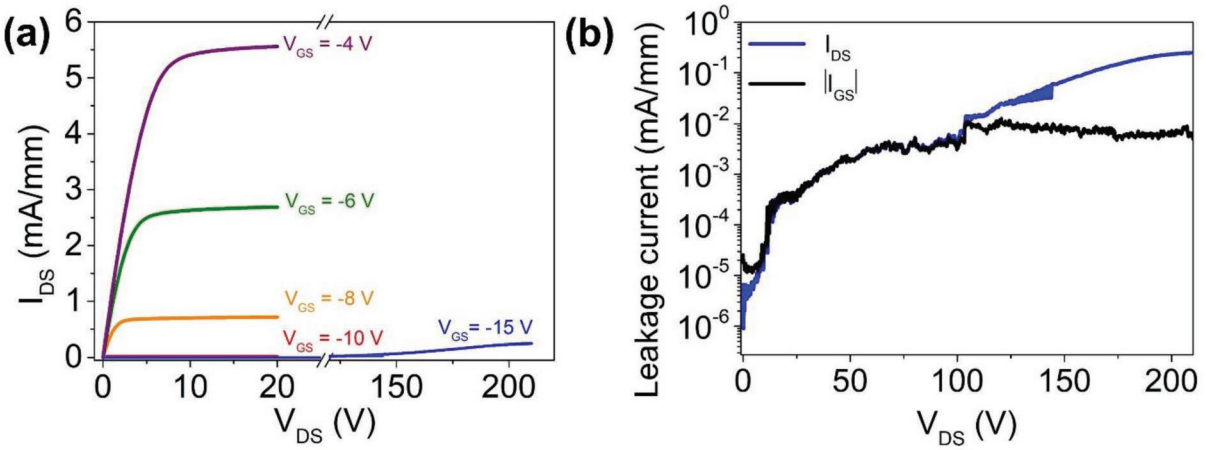

Figure 5. a) Three terminal off-state breakdown measurements of the fabricated TG β-Ga_2O_3 MESFET with floating BG at $V_{TG} = -15$ V. b) Comparison of the leakage current I_{DS} and I_{GS}.

enhanced up to 2.76 mS mm^{-1} as V_{DS} increases to 10 V as presented in I_{DS}–V_{GS}–g_m curves of Figure 6d. The positive ΔV_{TH} is ascribed to decreased effective channel thickness under double-gate modulation. Therefore, the thinner and more effectively gate-controlled channel layer results in the significantly improved carrier transport properties, which can be further enhanced by designing higher W/L as well as doping level.

3. Conclusion

In summary, we fabricate asymmetric double-gate (DG) β-Ga_2O_3 nanomembrane FET comprised of bottom-gated MOSFET and top-gated MESFET. Due to the excellent Schottky contact formed at Ni/β-Ga_2O_3 interface, as characterized by measuring the SBD, TG β-Ga_2O_3 MESFET

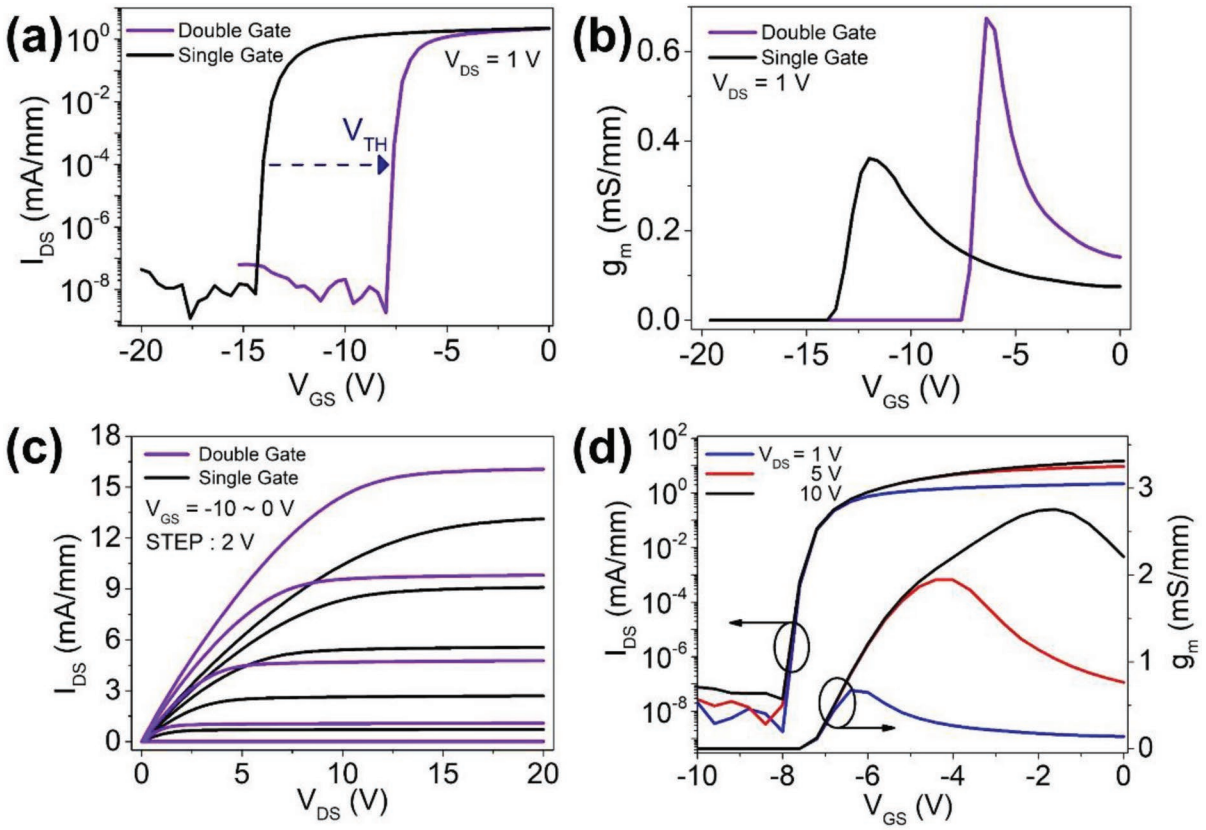

Figure 6. a) Positive shifted transfer curve ($\Delta V_{TH} = 6.1$ V), b) enhanced g_m (1.9 times), and c) increased drain-current (I_{DS}) of single TG modulation in comparison with double gate β-Ga_2O_3 FET (i.e., TG and BG simultaneously). d) I_{DS}–V_{GS}–g_m curves of the double gate β-Ga_2O_3 FET at various V_{DS} of 1, 5, and 10 V.

exhibits high on/off ratio, low subthreshold slope, and high transconductance with negligible hysteresis. In addition, the high breakdown voltage as anticipated by the three terminal off-state breakdown measurements is promising for power devices. On the basis of the energy band model supported by the simulation study, the asymmetric gate modulation is beneficial toward high-performance DG β-Ga_2O_3 nanomembrane FET. Consequently, positive-shifted threshold voltage, reduced subthreshold slope, almost two times enhanced transconductance, and 1.2 times increased mobility are achieved through DG operation. All these results suggest the proposed asymmetric DG β-Ga_2O_3 nanomembrane FET to be promising for energy-efficient high voltage and frequency device applications with further optimal material and structure co-designs.

4. Experimental Section

Device Fabrication and Characterization: Mechanically exfoliated β-Ga_2O_3 flakes from β-Ga_2O_3(-201) bulk substrate with unintentional n-type doping (UID) concentration of 4.8×10^{17} cm^{-3} (Tamura Corp., Japan) by a conventional scotch-tape method were transferred on to a heavily doped p-type Si substrate with thermally grown 300 nm SiO_2 layer. Then source and drain (S/D) electrodes of Ti/Au (20/80 nm) were deposited by thermal evaporation and patterned using a conventional photolithography and lift-off process. The channel length (L) between source and drain was 21.6 µm and width (W) was 7.1 µm. After that, a top-gate (TG) electrode of Ni/Au (20/80 nm) was deposited on the top of β-Ga_2O_3(100) channel layer by thermal deposition and then finished with the lift-off process. Electrical properties of the fabricated individual devices and double-gate operation were characterized by using semiconductor parameter analyzer (SCS-4200A, Keithley) in dark ambient conditions. The β-Ga_2O_3 channel thickness was measured by atomic force microscopy (AFM) (XE100, PSIA) and structural analysis was conducted using HR-TEM (Talos F200X).

TCAD Simulations: A commercial TCAD Sentaurus was used to study the fabricated device and to understand asymmetric gate modulation effect.[29,30] Standard β-Ga_2O_3 material parameters such as electron effective mass (m*) and conduction band density of state (N_c) were adopted at first. Then some of the parameters were calibrated to the experimental results; the model parameter β_0 (beta0) and saturation velocity (vsat0) for high-field dependence were set to be 0.4 and 1×10^8 cm s^{-1}, respectively. Ni/β-Ga_2O_3 interface was defined as a Schottky contact. Although the β-Ga_2O_3 channel was modeled with n-type doping concentration of 2.0×10^{17} cm^{-3}, which was lower than the nominal value of the initial bulk substrate, the thickness was set to be 150 nm in order to fully deplete the channel without modifying other parameters. Then a device mesh was constructed to match the fabricated asymmetric DG β-Ga_2O_3 FET and then perform electron-density (*eDensity*) simulation.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

asymmetric-gate, beta-gallium oxide, metal-semiconductor field-effect transistor, metal-oxide field-effect transistor

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